

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, TAUP0, M87

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

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25	25	SB Pwr Mgt, GPIO, Clink	T9_NAME	03/16/2007
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27	27	SB Decoupling	T9_NAME	01/17/2007
28	28	SB Misc	(T9_MLB)	08/24/2006
29	29	Clock (CK505)	T9_NAME	03/16/2007
30	30	Clock Termination	(MASTER)	08/23/2006
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32	32	DDR2 SO-DIMM Connector B	(M59_SYNC)	08/24/2006
33	33	Memory Active Termination	(T9_NAME)	11/14/2006
34	34	Left I/O Board Connector	(M59_SYNC)	08/24/2006
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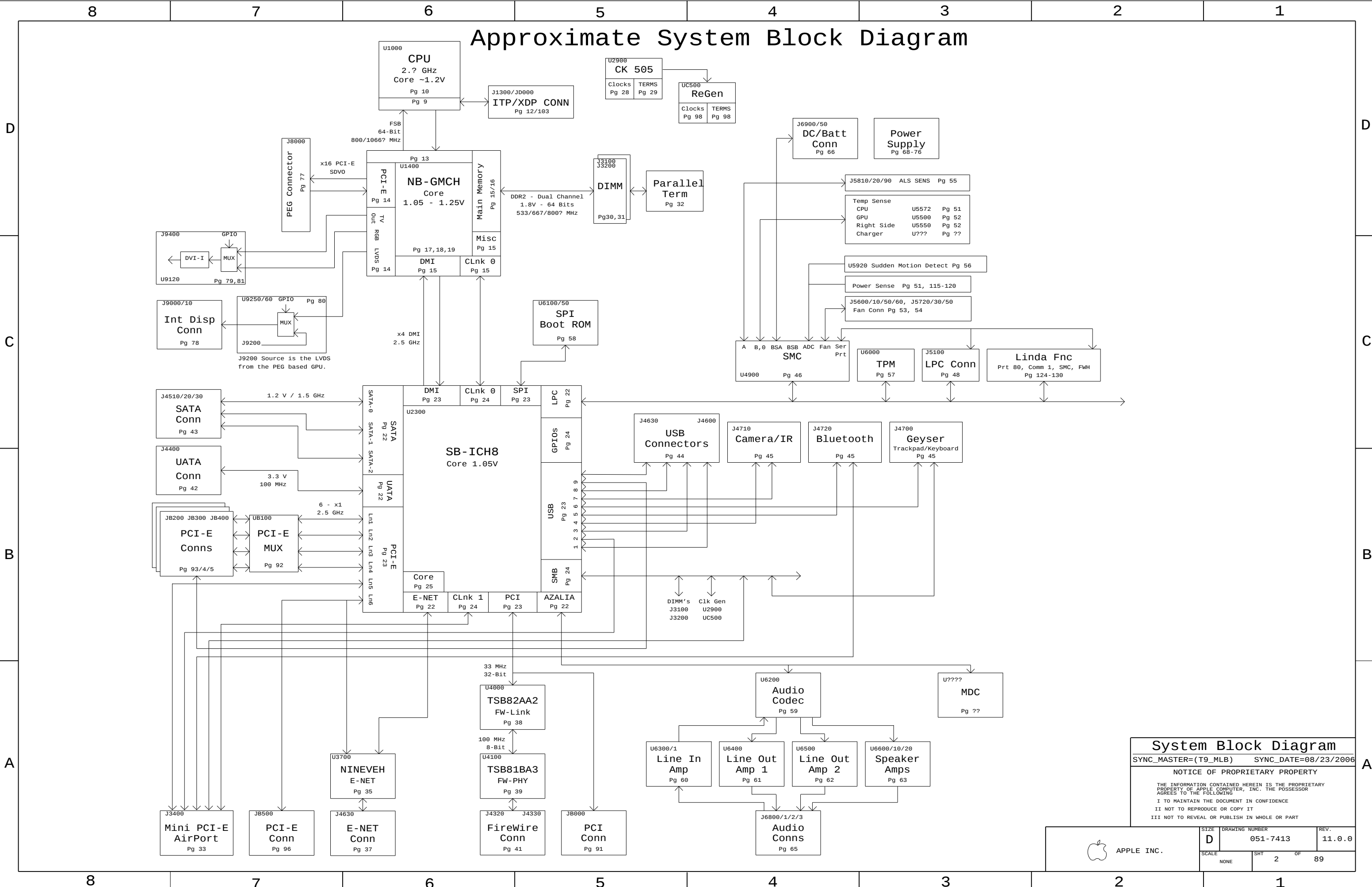
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56	PBus-In & Battery Connectors	(M59_SYNC)	09/09/2006
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62	1.5V Power Supply	M76_MLB	03/12/2006
63	FW PHY Power Supplies	M76_MLB	03/19/2006
64	3.425V G3Hot Supply & Power Control	M88	08/02/2006
65	NV G84M PCI-E	(MASTER)	(MASTER)
66	NV G84M Core/FB Power	(MASTER)	(MASTER)
67	NV G84M Frame Buffer I/F	(MASTER)	(MASTER)
68	GDDR3 Frame Buffer A (Top)	(MASTER)	(MASTER)
69	GDDR3 Frame Buffer B (Top)	(MASTER)	(MASTER)
70	NV G84M GPIO/MIO/Misc	(MASTER)	(MASTER)
71	GPU Straps	M88	08/02/2006
72	NV G84M Video Interfaces	(MASTER)	(MASTER)
73	GPU (G84M) Core Supply	M88	08/02/2006
74	LVDS Display Connector	(MASTER)	(MASTER)
75	GDDR3 Frame Buffer A (Bot)	M88_MLB_VRAM_BOT	06/19/2006
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87	GPU (G84M) Constraints	(MASTER)	(MASTER)
88	Project Specific Constraints	(MASTER)	(MASTER)
89	PCB Rule Definitions	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7413	1	SCHEM, TAUP0, M87	SCH	CRITICAL	
820-2249	1	PCBF, TAUP0, M87	PCB	CRITICAL	

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DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 12 18:10:11 2007
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DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING		METRIC <table><tr><td>DRAFTER</td><td>/</td><td>DESIGN CK</td><td>/</td></tr><tr><td>ENG APPD</td><td>/</td><td>MFG APPD</td><td>/</td></tr><tr><td>QA APPD</td><td>/</td><td>DESIGNER</td><td>/</td></tr><tr><td>RELEASE</td><td>/</td><td>SCALE</td><td>NONE</td></tr></table> MATERIAL/FINISH NOTED AS APPLICABLE SIZE D		DRAFTER	/	DESIGN CK	/	ENG APPD	/	MFG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	NONE	 APPLE INC. NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE IT IS NOT TO REPRODUCE OR COPY IT IT IS NOT TO REVEAL OR PUBLISH IN WHOLE OR PART TITLE SCHEM, TAUP0, M87 <table><tr><td>DRAWING NUMBER</td><td>051-7413</td><td>REV.</td><td>11.0.6</td></tr><tr><td colspan="2">SHT</td><td>1</td><td>OF 89</td></tr></table>		DRAWING NUMBER	051-7413	REV.	11.0.6	SHT		1	OF 89
DRAFTER	/	DESIGN CK	/																										
ENG APPD	/	MFG APPD	/																										
QA APPD	/	DESIGNER	/																										
RELEASE	/	SCALE	NONE																										
DRAWING NUMBER	051-7413	REV.	11.0.6																										
SHT		1	OF 89																										
 THIRD ANGLE PROJECTION																													



System Block Diagram

SYNC_MASTER=(T9_MLB)

SYNC_DATE=08/23/2006

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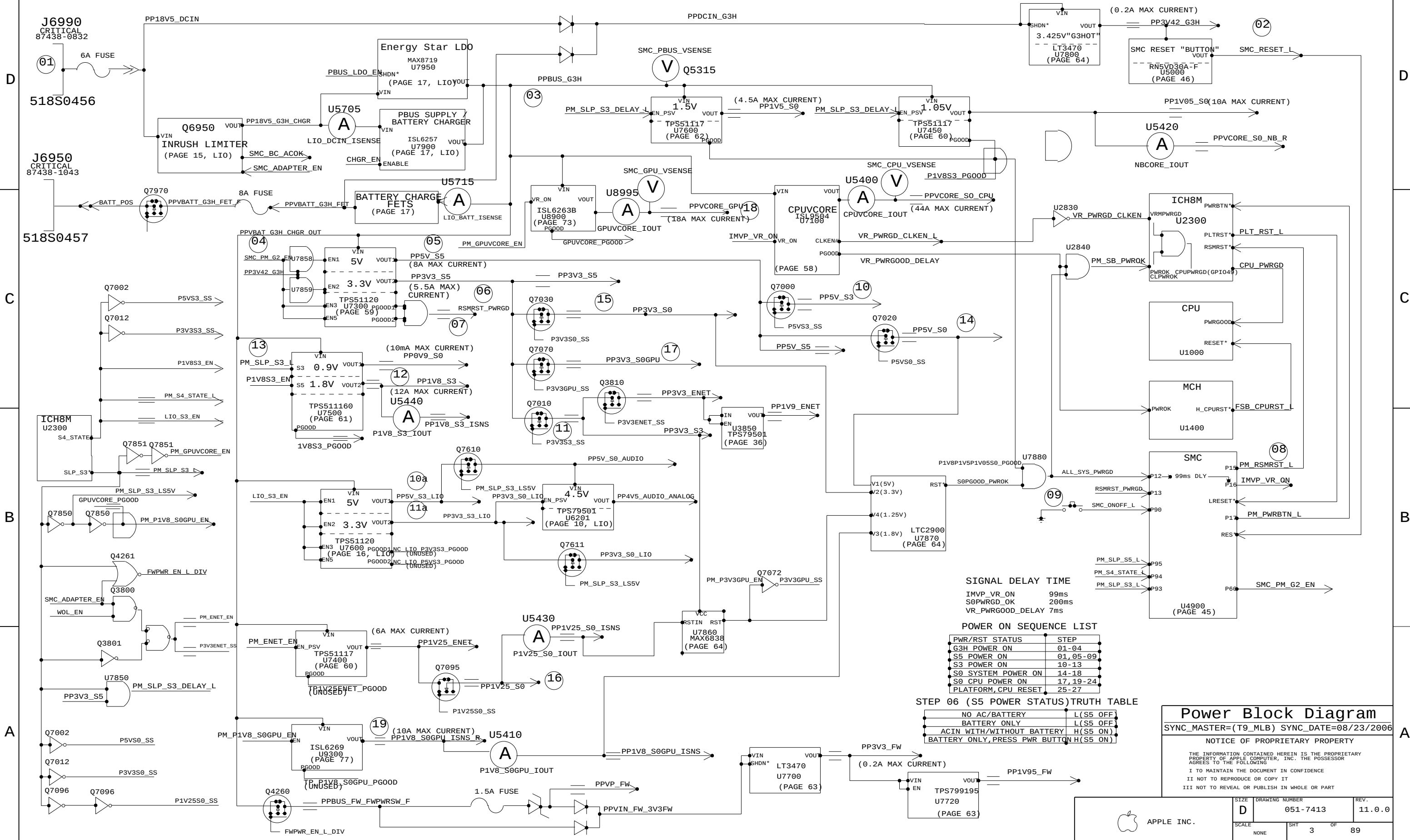
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M87 POWER SYSTEM ARCHITECTURE



Power Block Diagram

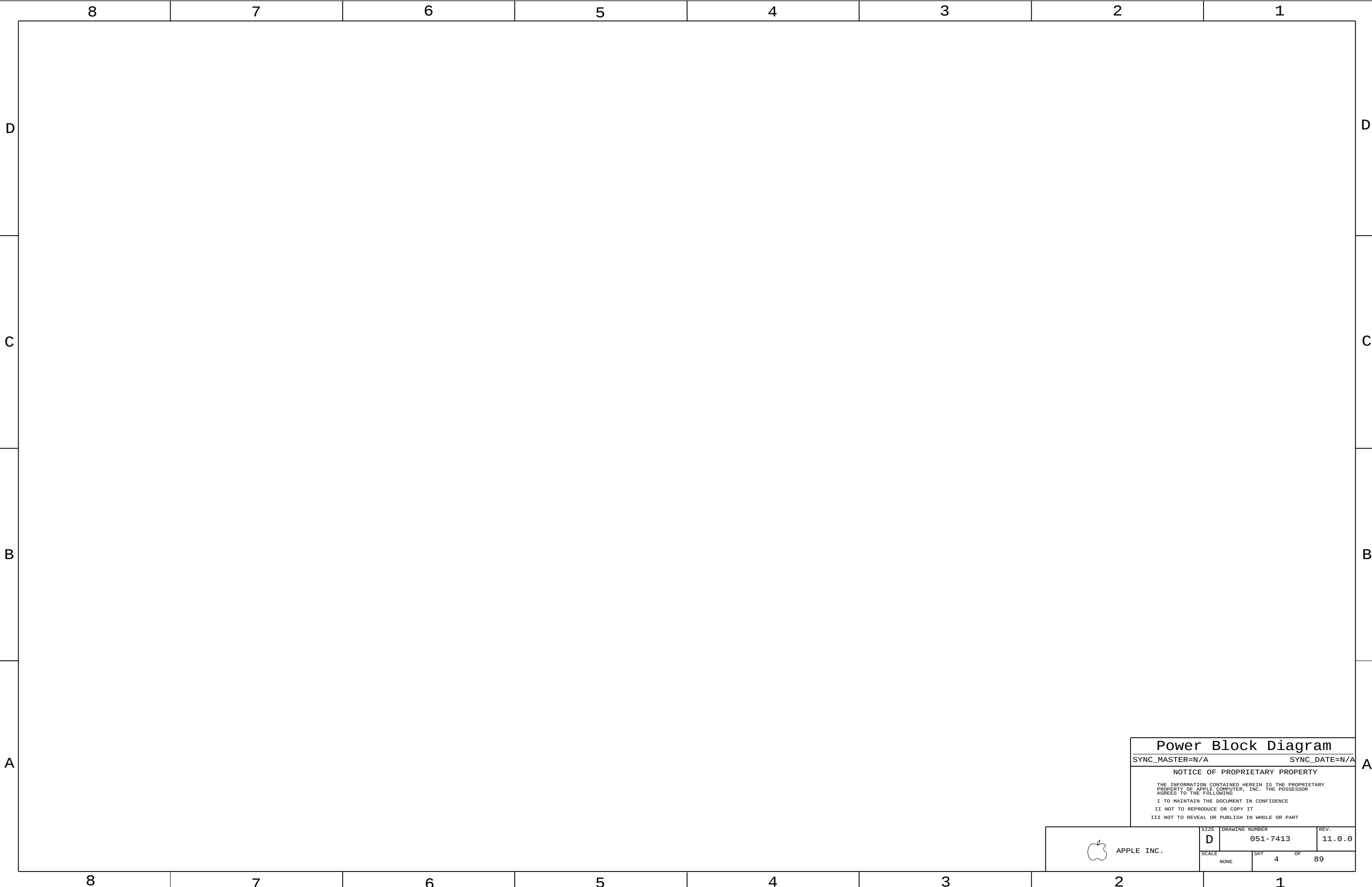
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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	3	89



Power Block Diagram			
SYNC_MASTER=N/A		SYNC_DATE=N/A	
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 4 OF 89	

	8	7	6	5	4	3	2	1	
D	PROTO 0.1.0: 04/26/07 -- Design branched from 051-7225-A 04/26/07 -- Clock Termination: Removed support for SLG8LP537 device (GPU_CLK_27M/27MSS muxes, etc) 04/26/07 -- Clock Termination: Added S0-powered AND gate between GPU_PG00D and SLG2AP101 enable pin to eliminate leakage path (rdar://5086613) 04/26/07 -- SB Misc: Removed EXTGPU_RST_L support for resetting the GPU (hardware control only) 04/26/07 -- Power Control: Removed U7858 and R7860. Tied SMC_PM_G2_EN/PM_G2_EN directly to S5 regulators 04/26/07 -- SB Decoupling: Replaced L2700 with 155S0333 for AVL updates 04/26/07 -- FW Port Power: Replaced D4260 with proper symbol (instead of table) 04/30/07 -- FW Port Power: Updated U4210 to 353S1744 for AVL updates 05/01/07 -- Current Sensors: Changed R5425/35/45 to RES_SENSE symbol which implements kelvin sensing without the need for XW shorts 0.1.2: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100) 05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253) 0.2.0: 05/10/07 -- Thermal Sensors: Added SIGNAL_MODEL=EMPTY properties to thermal sense diff pairs (rdar://5192397) 05/10/07 -- Current Sensors: Added SIGNAL_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397) 0.3.0: 05/14/07 -- Power Control: Added U7858,U7859 to properly enable/disable S5 regulators (rdar://TBD) 05/14/07 -- 5V/3.3V Regulators: Added C7307,C7308 to allow soft-start control of S5 regulators (rdar://TBD) 0.4.0: 05/22/07 -- Power Control: Added C7858 to decouple U7858/59 05/22/07 -- GPU Vcore: Removed Power Control circuitry 05/22/07 -- GPU Straps: Added R8734 to get PCIDEVID3 pullup 0.5.0: 06/06/07 -- GPU FB: Reassigned CS1/BA2 for future memory expansion 06/06/07 -- GPU FB: Changed 22uF, 0805 caps to 10uF, 0603 for future memory expansion 06/06/07 -- GPU FB: Reworked/added FB device Vrefs (with smaller FETs) for future memory expansion 06/06/07 -- Left Clutch I/C: Removed SIM I/F connector 0.6.0: 06/07/07 -- GPU Straps: U8700 changed to TS3V340 only 06/18/07 -- GPU FB: Added support for 1Gb density ICs (added MA<12> and CS1) 06/18/07 -- Left Clutch I/C: Added alternate camera connections (CCP2 I/F) 06/18/07 -- DFM: Added NC nets to allow copper on BGA corner balls (CPU and GPU) 06/19/07 -- GPU FB: Added 4 more 16Mx32 VRAM devices 06/20/07 -- Muxed Gfx: Began removing support for this feature 0.7.0: 06/25/07 -- GPU VCORE: U8900 Changed to IMVP6 06/25/07 -- FB REGULATOR: Added U9300 06/25/07 -- Muxed Gfx: Removed LVDS/BKLT muxes and support 06/25/07 -- Power Fet: Removed 1V8 and 1V25 Fets 06/25/07 -- Current Sense: Removed U5410 NBGfx Sense 06/25/07 -- Regulators: Changed Q7320,Q7360,Q7410,Q7460,Q7620 to SI7110N 0.8.0: 06/27/07 -- Power Fet: Removed 1v8 S0 Fet, cleaned up aliasing 0.9.0: 06/27/07 -- Current Sense: Added 1v8 FB current sense 06/27/07 -- GPU VCORE: Added additional High side Input Cap 0.10.0: 06/27/07 -- MUX Gfx: Delete GPU PG00D Monitor 0.11.0: 06/27/07 -- Aliasing:Cleanup 06/27/07 -- BOM: Changed BOM option table for M87 0.12.0: 07/02/07 -- Power CTL:Added 1.25 PG00D/3V3 GPU EN,Moved 1V8_S3 to pgood chain 07/02/07 -- LCC: Added Camera/MIC pins 07/02/07 -- DVI: Removed SB Hotplug Detect support(muxed gfx) 0.13.0: 07/05/07 -- Aliasing: Moved pages back in sync with T9, aliasing now on separate page 07/05/07 -- Regulators: Changed L7100,L7101 to 4mm 152S0433 1.2.0: 08/02/07 -- USB: Change to active enable USB ports 08/02/07 -- Regulators: Changed U8900 to use VID instead of Feedback resistors								D
C									C
B	EVT 4.1.0: 08/09/07 -- Current Sense: Change Q5322 TO FDN337 to accommodate TH1H 08/09/07 -- Ethernet: Change T3900,T3901 to 157S0053 5.1.0: 08/13/07 -- Regulators: Change GPUVCORE VID pullup/pulldowns to 2.2K DVT 10.0.0: 09/21/07 -- BOM OPTION: Add 2.4Ghz 256MB VRAM Config, change 2.5Ghz Conifgs to 512MB VRAM								B
A									A
	8	7	6	5	4	3	2	1	

Revision History

SYNC_MASTER=N/A

SYNC_DATE=N/A

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SIZE
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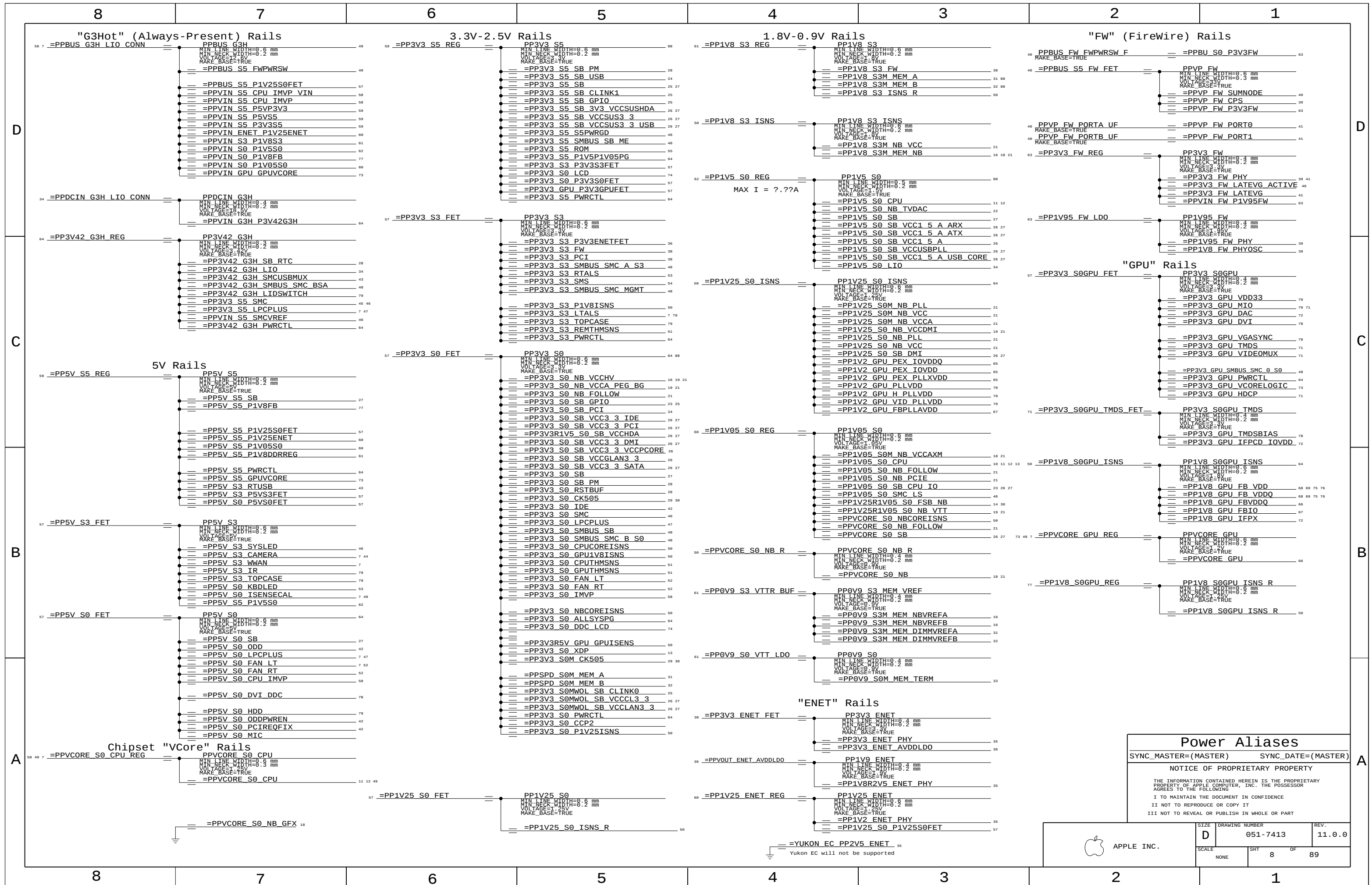
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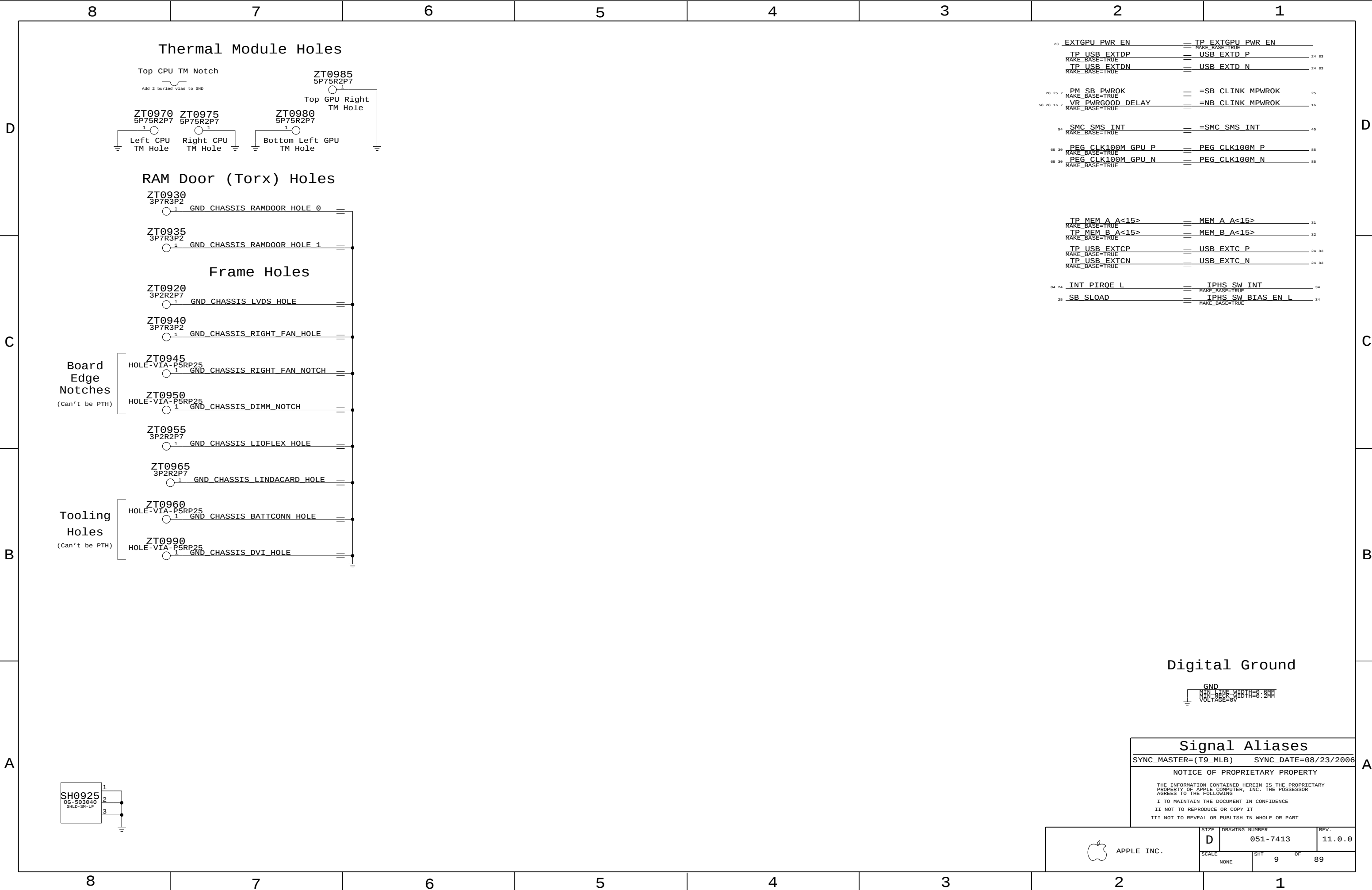
REV.
11.0.0

SCALE
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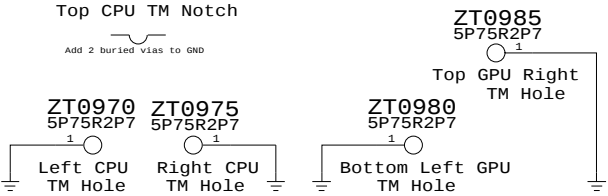
SHT
6

OF
89

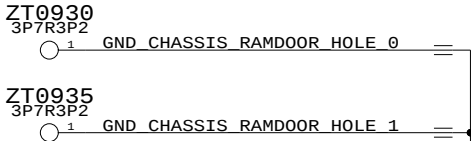




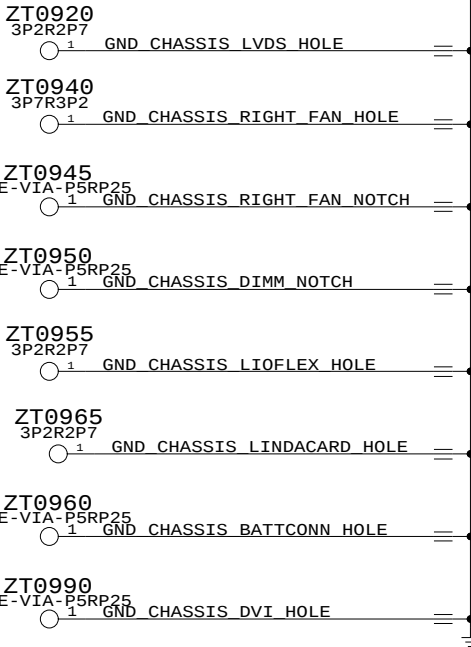
Thermal Module Holes



RAM Door (Torx) Holes



Frame Holes



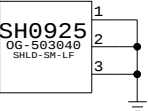
Board Edge Notches

(Can't be PTH)

Tooling Holes

(Can't be PTH)

Digital Ground



Signal Aliases

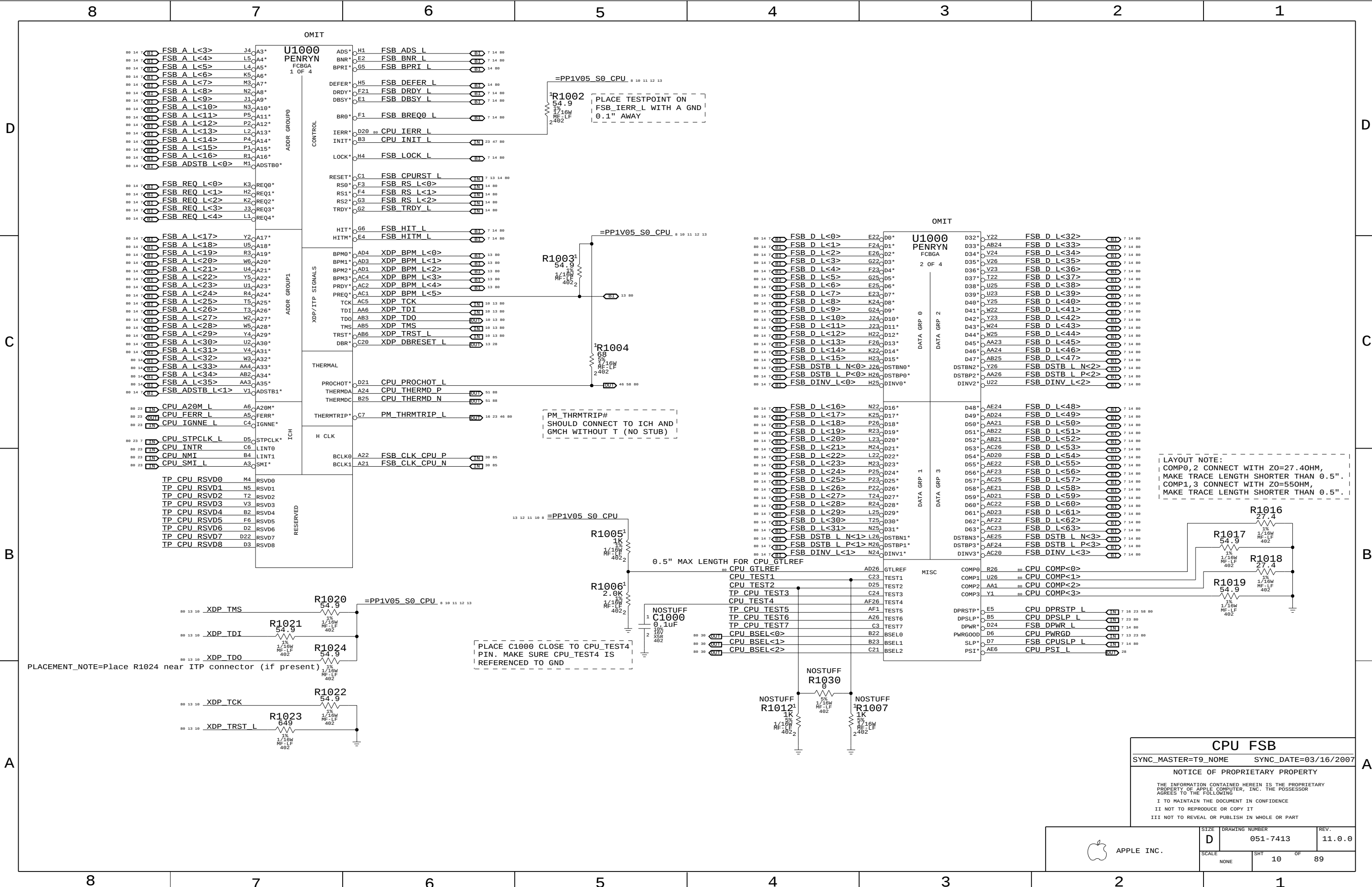
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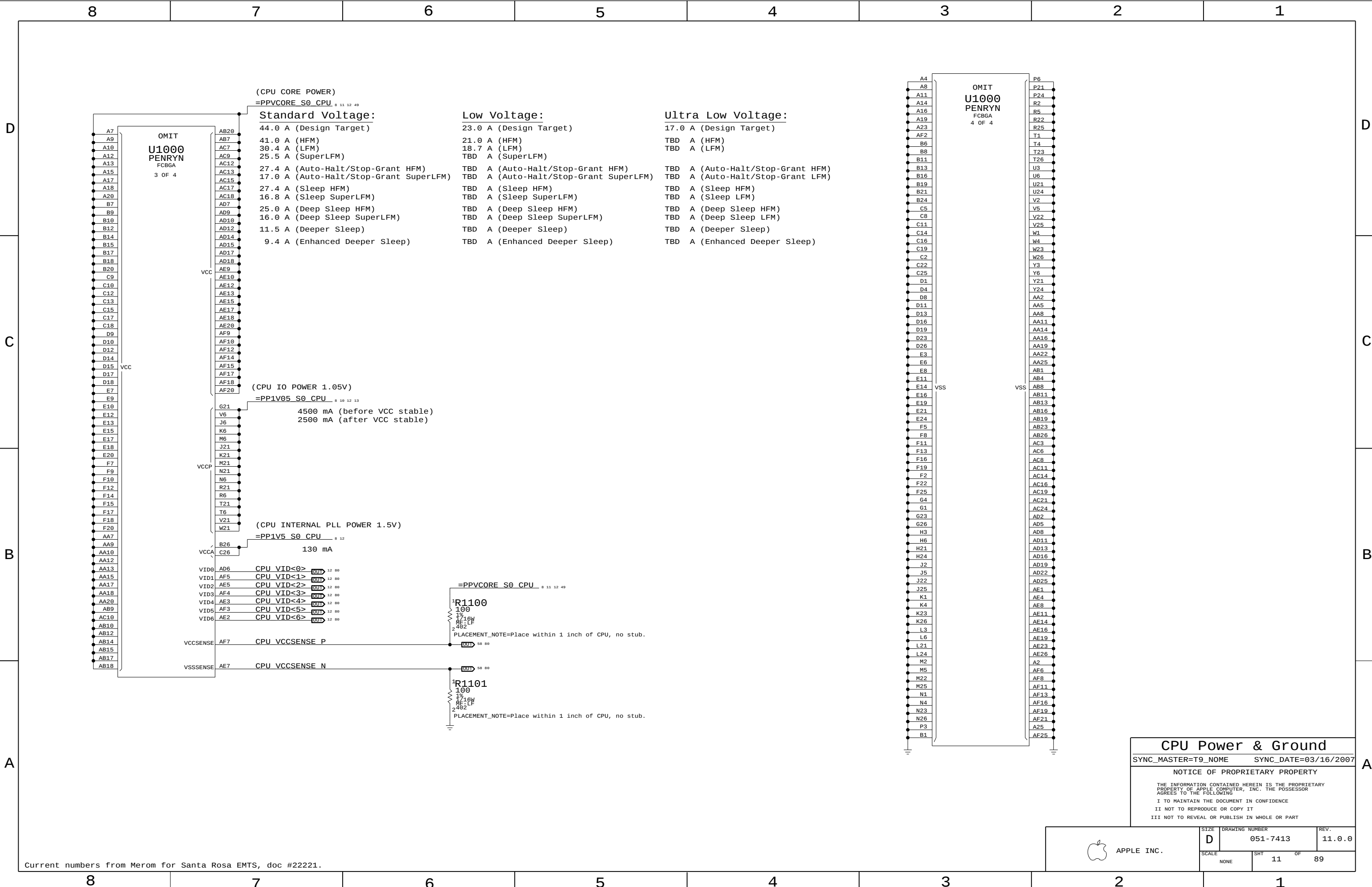
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SCALE	NONE	SHT	9	OF	89





(CPU CORE POWER)

=PPVCORE S0 CPU 8 11 12 49

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)

=PP1V05 S0 CPU 8 10 12 13

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5 S0 CPU 8 12

130 mA

VID0	AD6	CPU VID<0>	12 80
VID1	AF5	CPU VID<1>	12 80
VID2	AE5	CPU VID<2>	12 80
VID3	AF4	CPU VID<3>	12 80
VID4	AE3	CPU VID<4>	12 80
VID5	AF3	CPU VID<5>	12 80
VID6	AE2	CPU VID<6>	12 80

VCCSENSE AF7 CPU VCCSENSE P

VSSSENSE AE7 CPU VCCSENSE N

=PPVCORE S0 CPU 8 11 12 49
R1100
100
1%
10W
06-1F
2462
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
10W
06-1F
2462
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

CPU Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

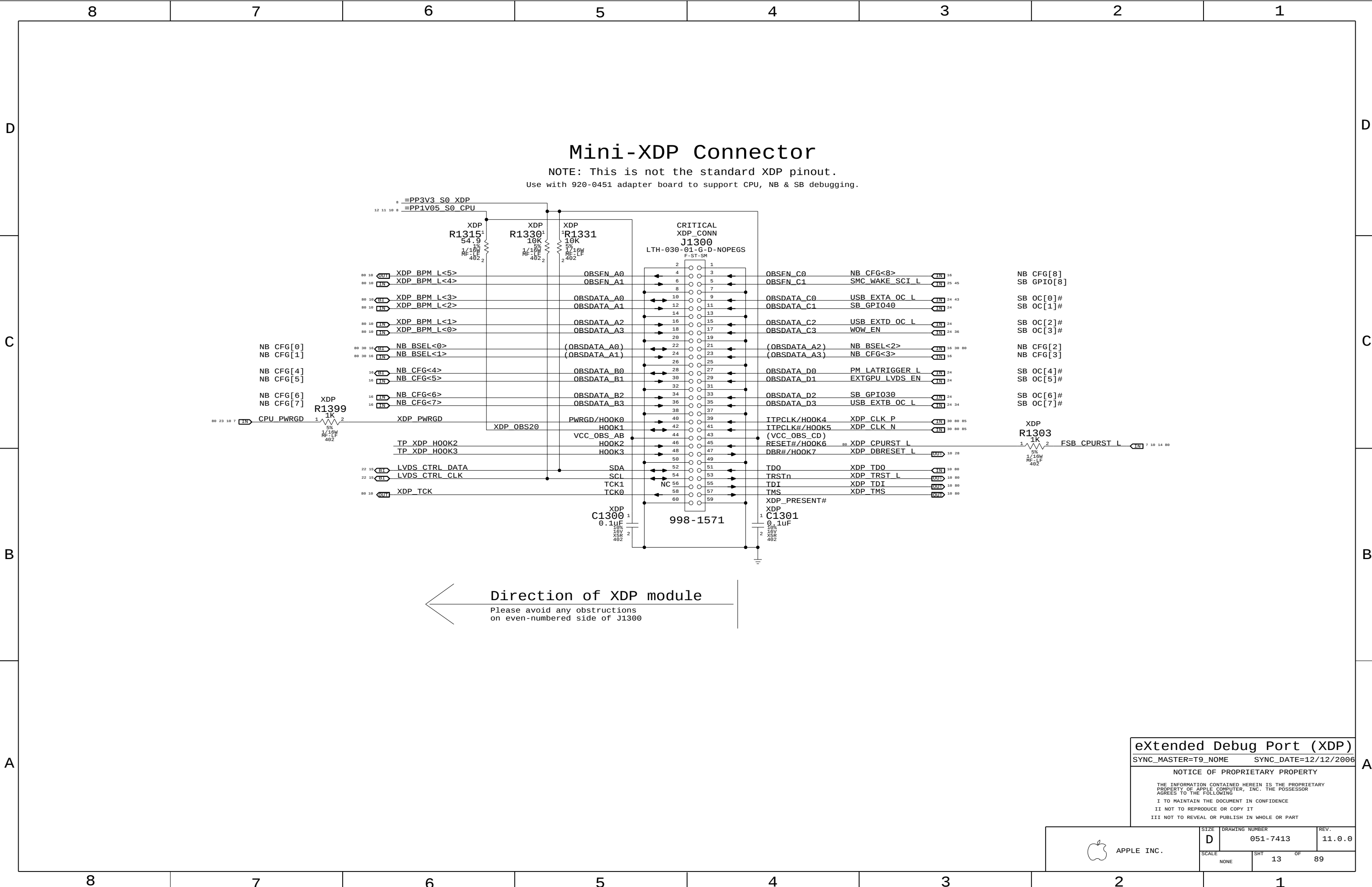
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D	051-7413	11.0.0
SCALE	SHT	OF
NONE	11	89



eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

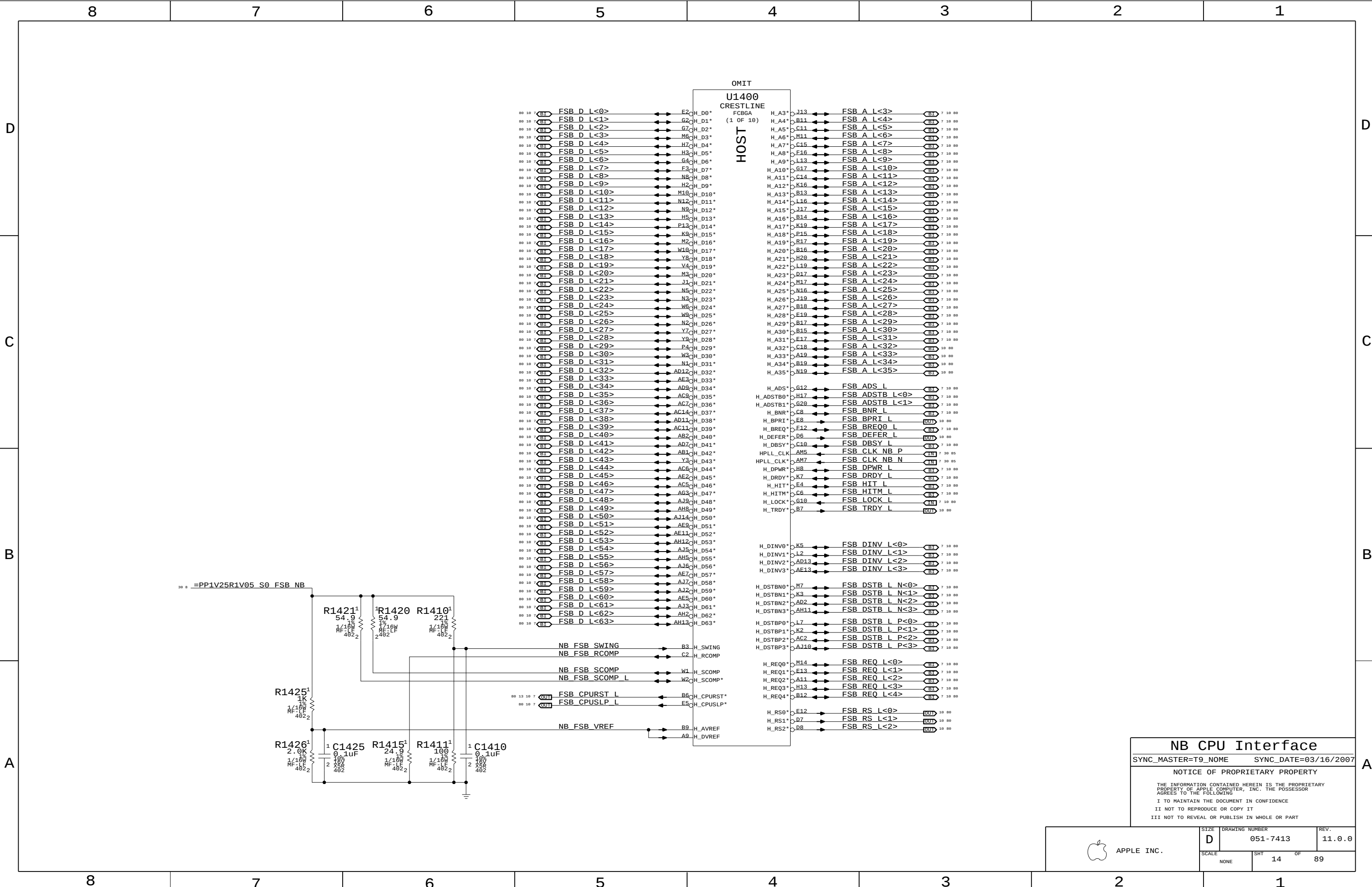
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SCALE	SHT	OF
NONE	13	89



NB CPU Interface

SYNC_MASTER=T9_NOME

SYNC_DATE=03/16/2007

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 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7413		11.0.0
SCALE		SHT	14	OF 89
NONE				

D

C

B

A

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

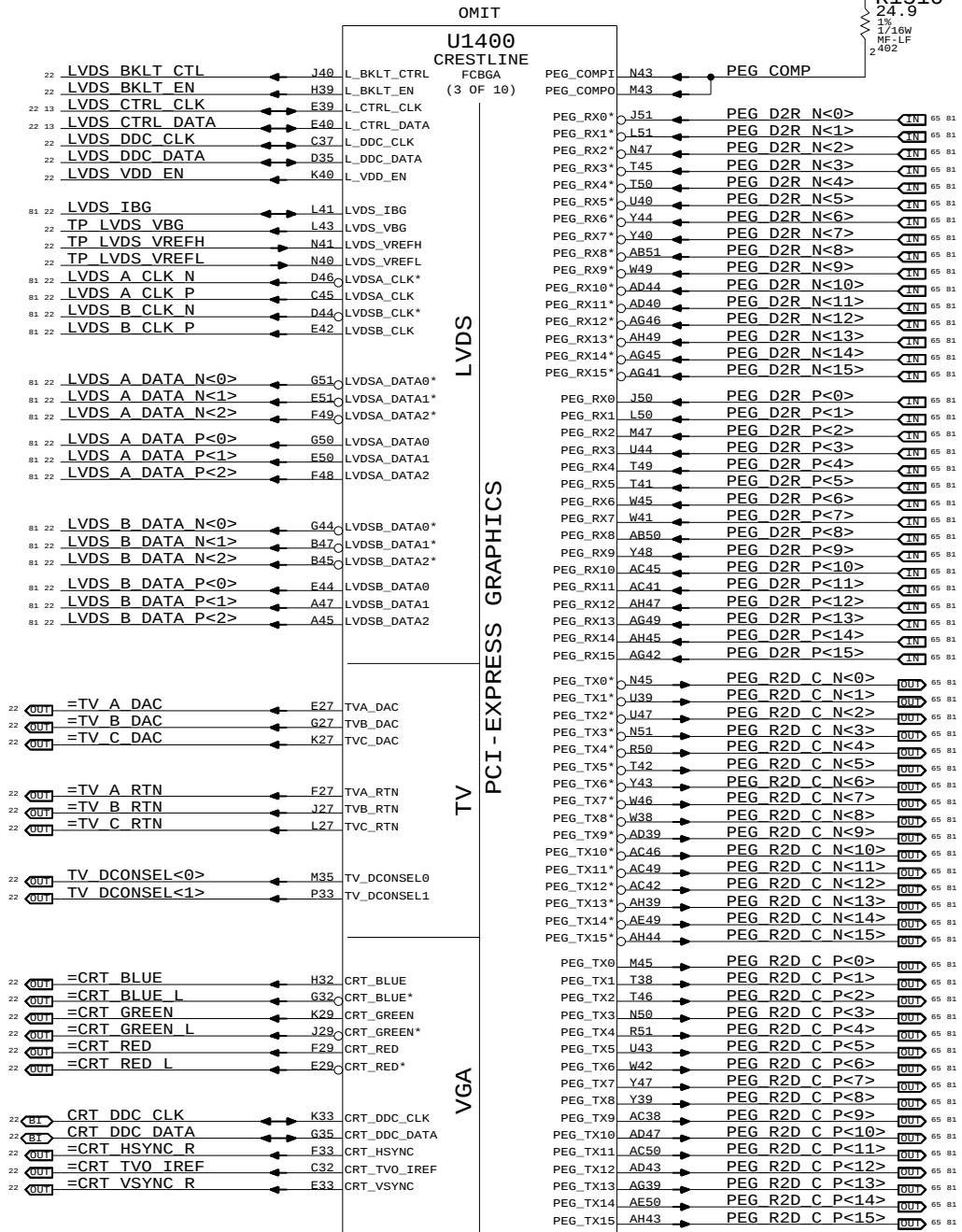
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TV0_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

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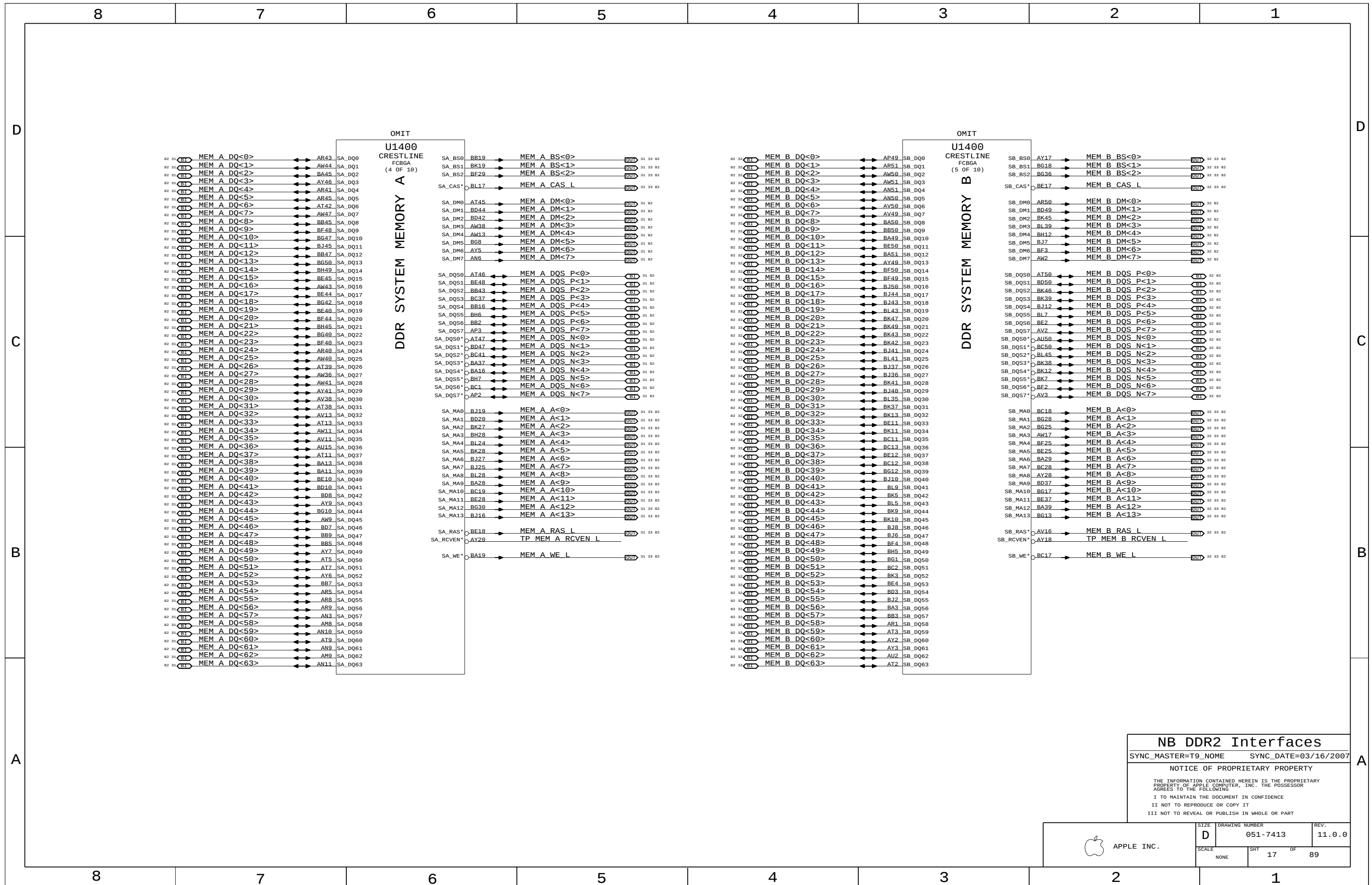
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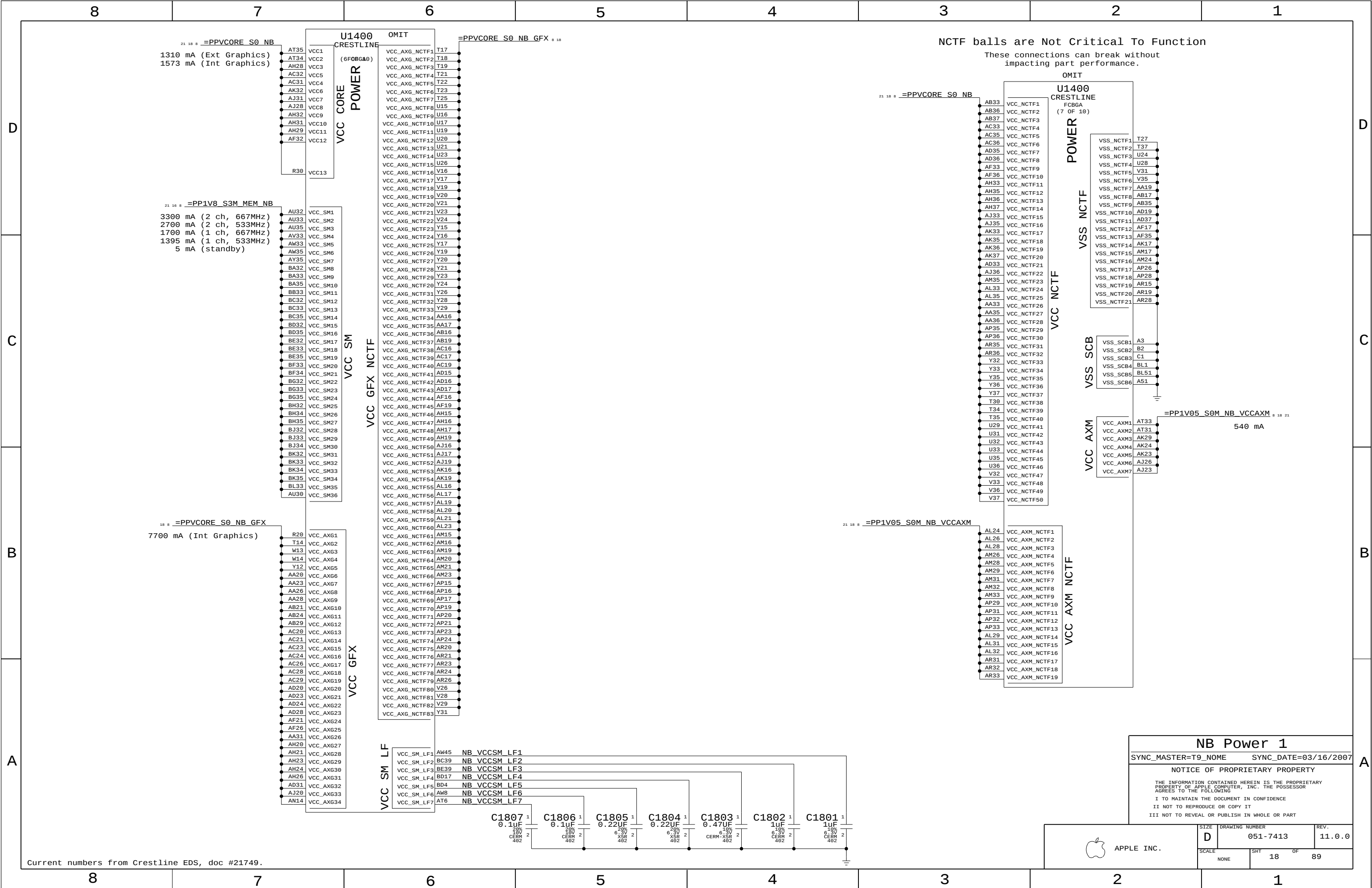
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SCALE	SHT	OF
NONE	15	89

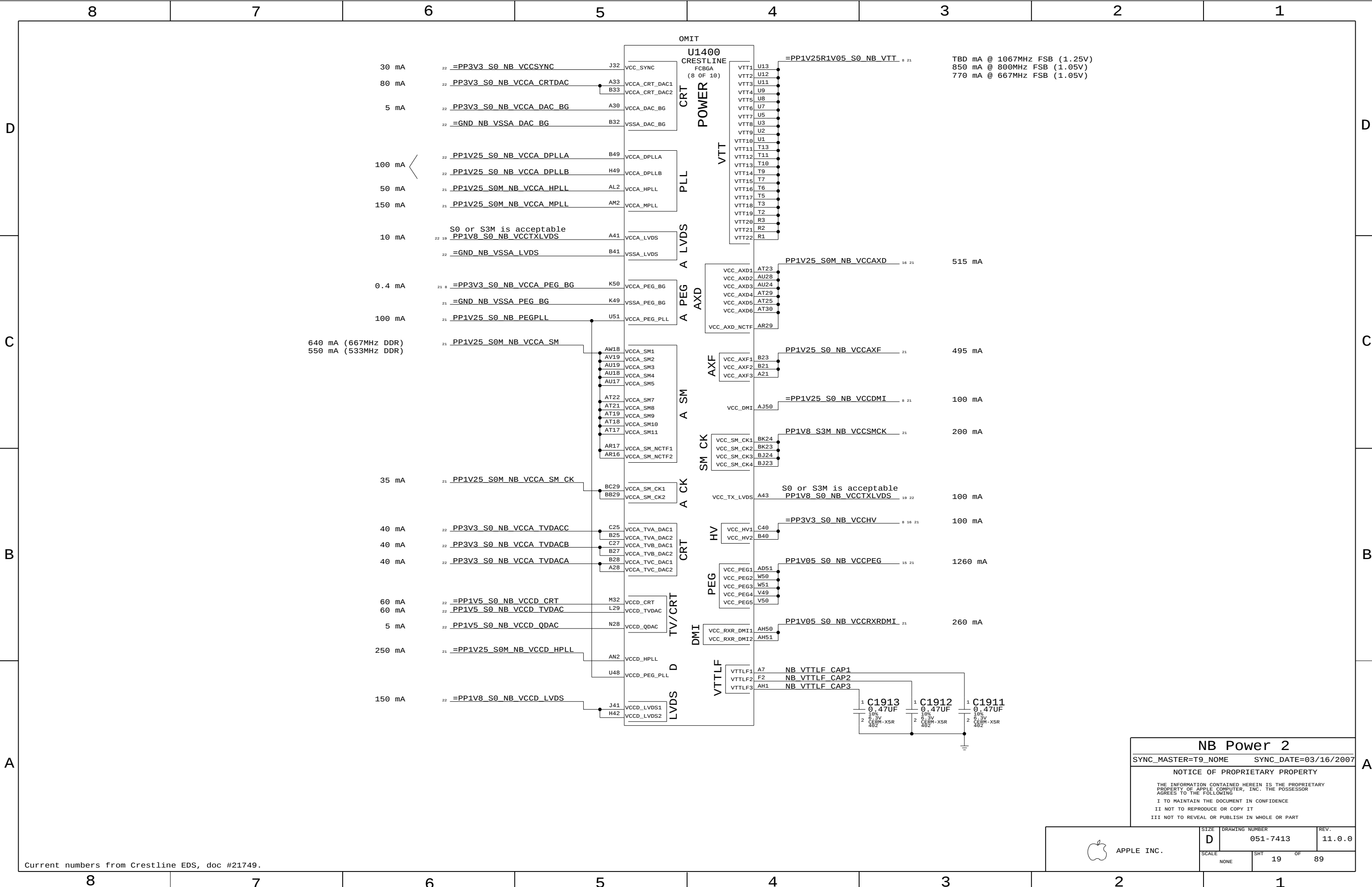




NCTF balls are Not Critical To Function
These connections can break without
impacting part performance.

NB Power 1
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	SCALE NONE	SHT 18	OF 89



NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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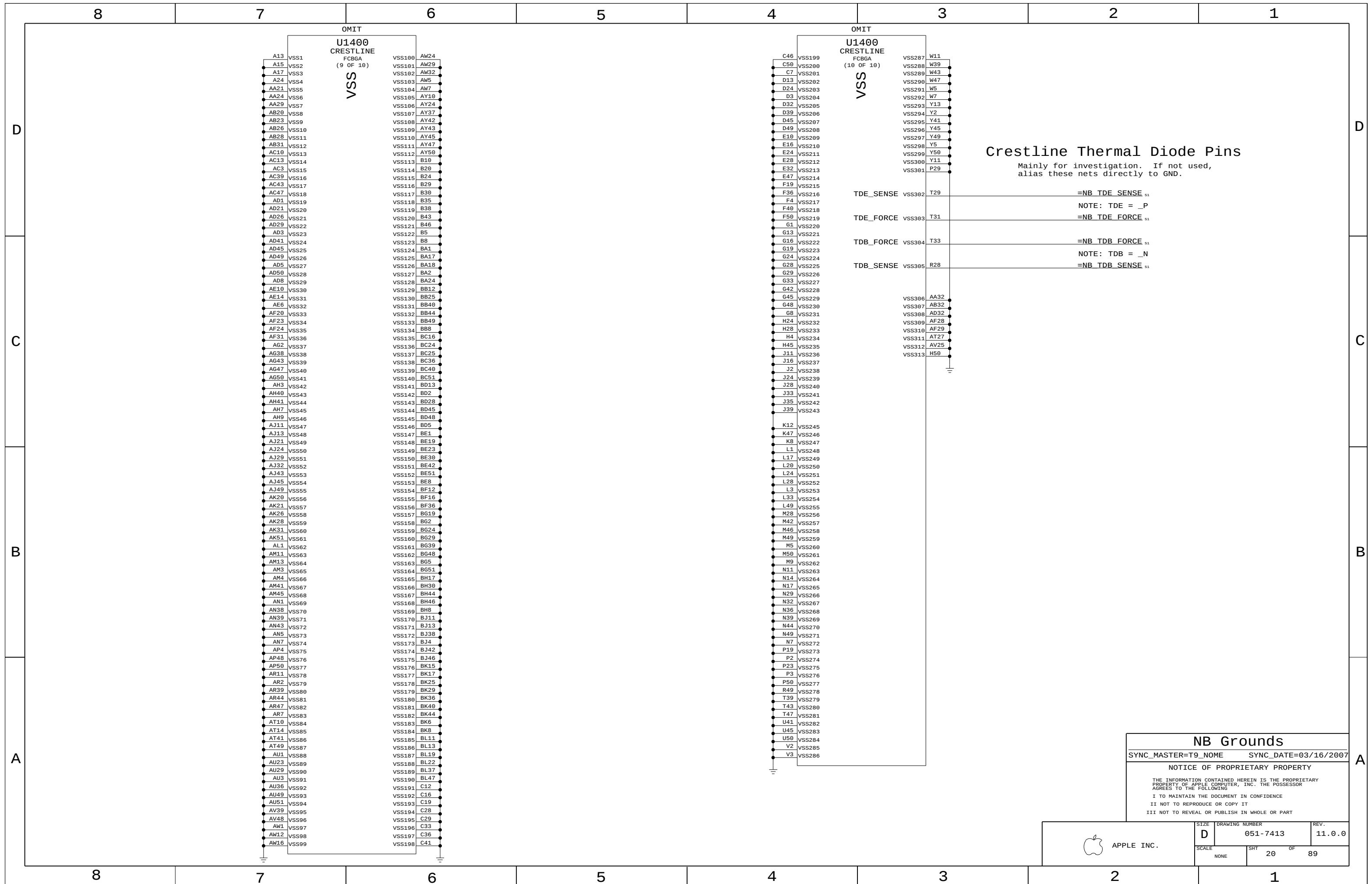
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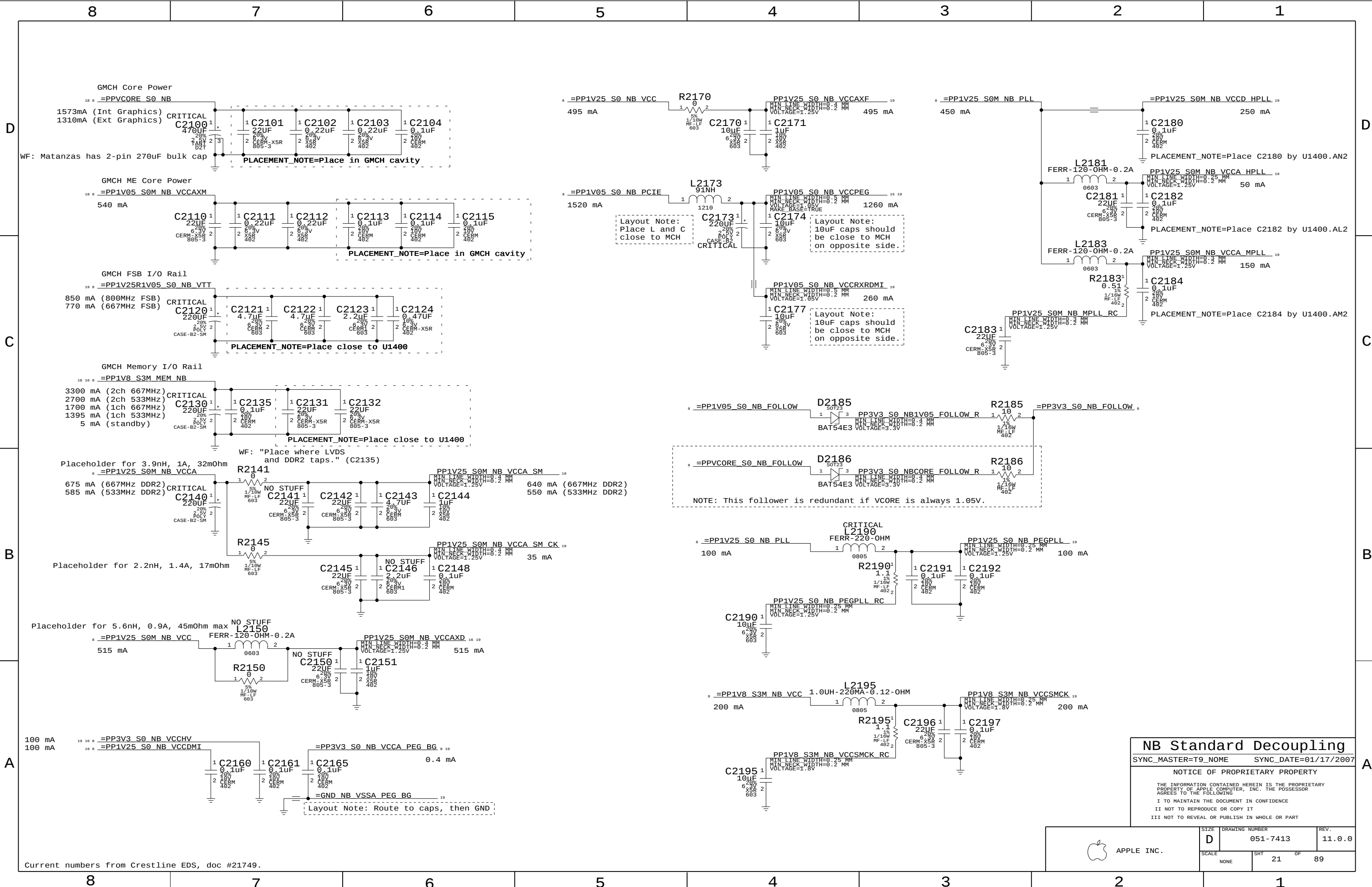
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NONE		19	89





NB Standard Decoupling

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SYNC_DATE=01/17/2007

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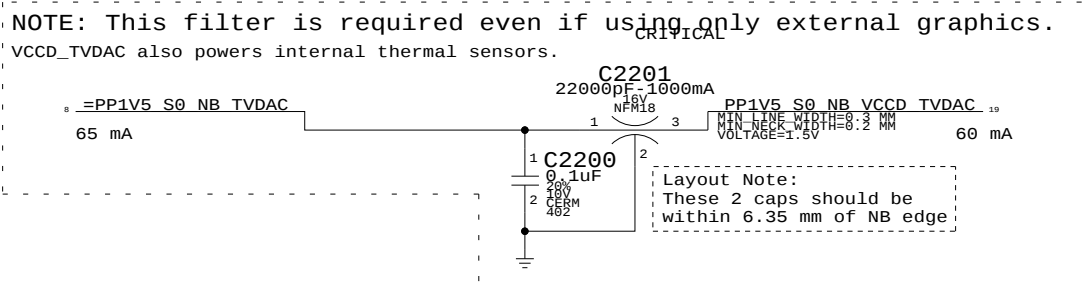
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	NONE	21	89

Crestline LVDS Strapping



Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

```

15 LVDS DDC CLK
15 LVDS DDC DATA
13 LVDS CTRL CLK
13 LVDS CTRL DATA
15 =CRT RED
15 =CRT RED L
15 =CRT GREEN
15 =CRT GREEN L
15 =CRT BLUE
15 =CRT BLUE L
15 =CRT HSYNC R
15 =CRT VSYNC R
15 =CRT TVO IREF
15 =TV A DAC
15 =TV A RTN
15 =TV B DAC
15 =TV B RTN
15 =TV C DAC
15 =TV C RTN
15 CRT DDC CLK
15 CRT DDC DATA
15 SDVO CTRLCLK
15 SDVO CTRLDATA
15 TV DCONSEL<0>
15 TV DCONSEL<1>
15 =NB CLK96M DOT N
15 =NB CLK96M DOT P
15 =NB CLK100M DPPLLSS P
15 =NB CLK100M DPPLLSS N

```

```

--GND NB_VSSA LVDS
PP1V8_S0 NB_VCC7XLVDS
PP1V25_S0 NB_VCCA DPLL
PP1V25_S0 NB_VCCA DPLLA
--PP1V8_S0 NB_VCCD LVDS
--PP1V5_S0 NB_VCCD CRT
PP3V3_S0 NB_VCCA CRTDAC
--PP3V3_S0 NB_VCCSYNC
PP1V5_S0 NB_VCCD QDAC
PP3V3_S0 NB_VCCA DAC_BG
--GND NB_VSSA DAC_BG
PP3V3_S0 NB_VCCA TVDAC
PP3V3_S0 NB_VCCA TVDACB
PP3V3_S0 NB_VCCA TVDACCC

```

15	<u>LVDS BKLT CTL</u>	<u>NC LVDS BKLT CTL</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS BKLT EN</u>	<u>NC LVDS BKLT EN</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS VDD EN</u>	<u>NC LVDS VDD EN</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS IBG</u>	<u>NC LVDS IBG</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VBG</u>	<u>NC LVDS VBG</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS A CLK N</u>	<u>NC LVDS A CLKN</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A CLK P</u>	<u>NC LVDS A CLKP</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B CLK N</u>	<u>NC LVDS B CLKN</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B CLK P</u>	<u>NC LVDS B CLKP</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA N<0></u>	<u>NC LVDS A DATAN<0></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS A DATA N<1></u>	<u>NC LVDS A DATAN<1></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA N<2></u>	<u>NC LVDS A DATAN<2></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<0></u>	<u>NC LVDS A DATAP<0></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<1></u>	<u>NC LVDS A DATAP<1></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<2></u>	<u>NC LVDS A DATAP<2></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA N<0></u>	<u>NC LVDS B DATAN<0></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS B DATA N<1></u>	<u>NC LVDS B DATAN<1></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA N<2></u>	<u>NC LVDS B DATAN<2></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS B DATA P<0></u>	<u>NC LVDS B DATAP<0></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA P<1></u>	<u>NC LVDS B DATAP<1></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
81 15	<u>LVDS B DATA P<2></u>	<u>NC LVDS B DATAP<2></u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VREFH</u>	<u>NC LVDS VREFH</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VREFL</u>	<u>NC LVDS VREFL</u>
		MAKE_BASE=TRUE NO_TEST=TRUE
16	<u>GFX VID<1></u>	<u>TP GFX VID<1></u>
		MAKE_BASE=TRUE
16	<u>GFX VID<2></u>	<u>TP GFX VID<2></u>
		MAKE_BASE=TRUE
16	<u>GFX VID<3></u>	<u>TP GFX VID<3></u>
		MAKE_BASE=TRUE
16	<u>GFX VID<4></u>	<u>TP GFX VID<4></u>
		MAKE_BASE=TRUE
16	<u>=GFX VR_EN</u>	<u>TP GFX VR_EN</u>
		MAKE_BASE=TRUE

Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB	SYNC_DATE=03/12/2007
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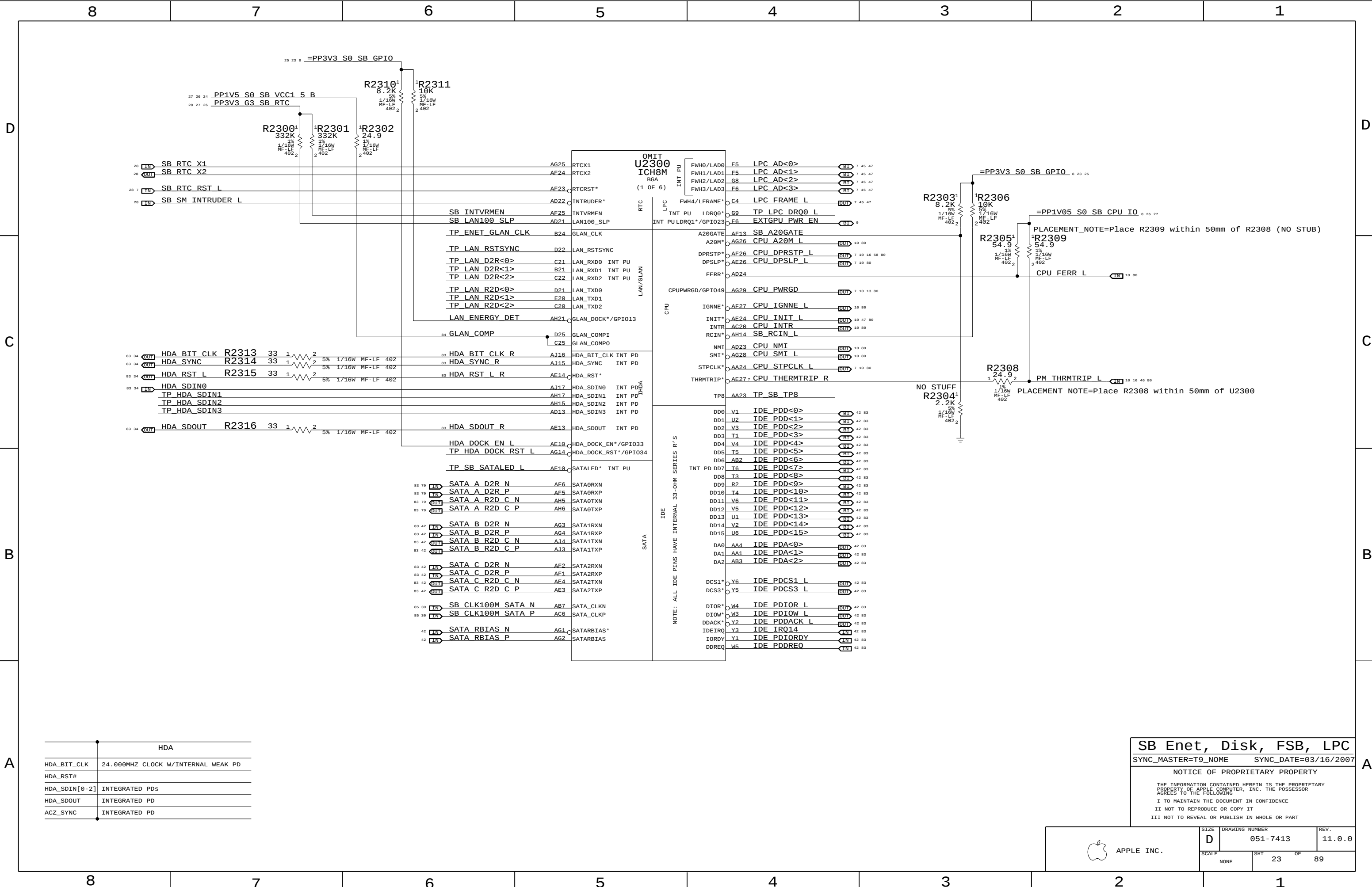
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HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDS
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

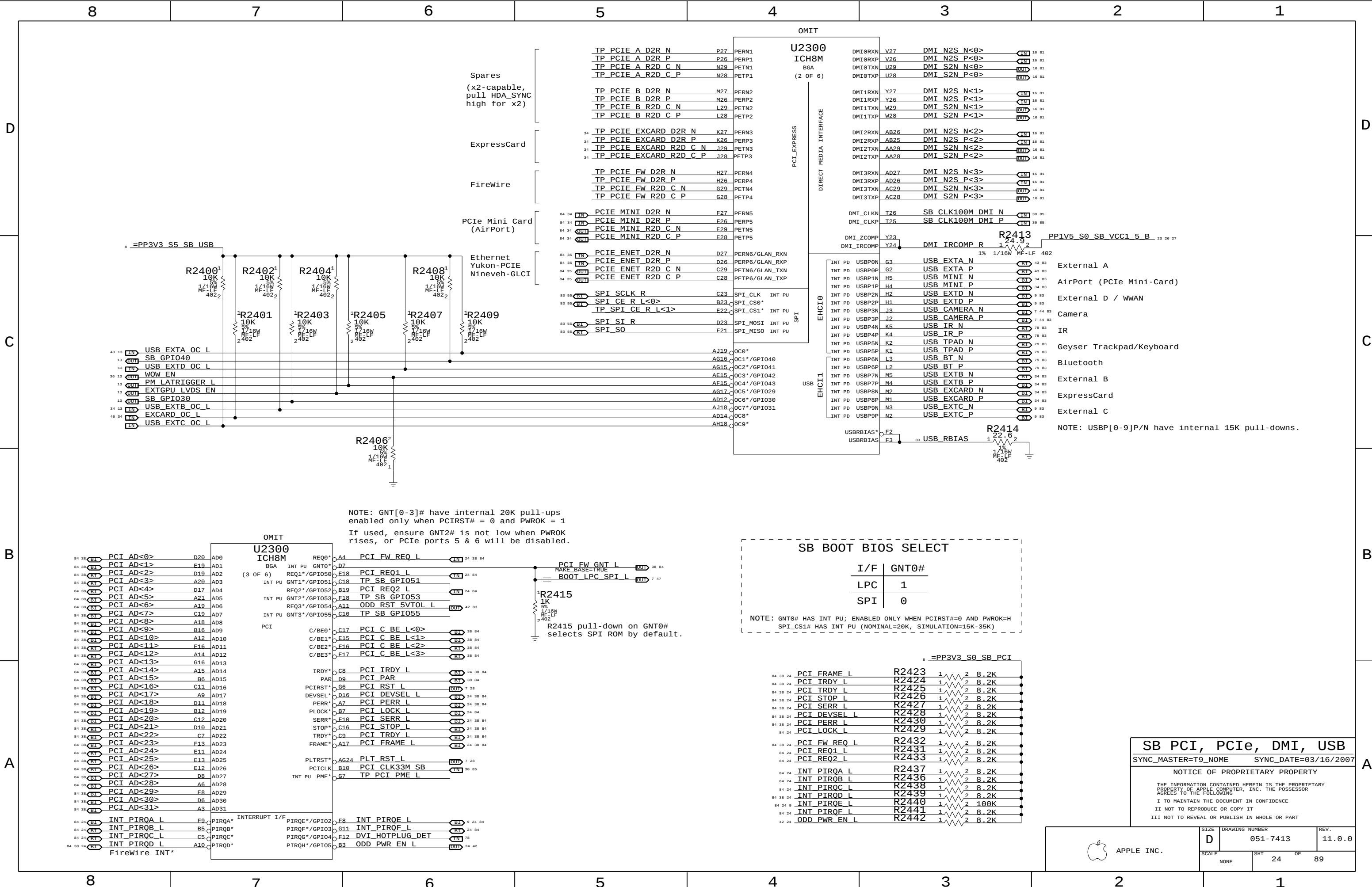
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NONE	23	89



NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

SB BOOT BIOS SELECT		
I/F	GNT0#	
LPC	1	
SPI	0	

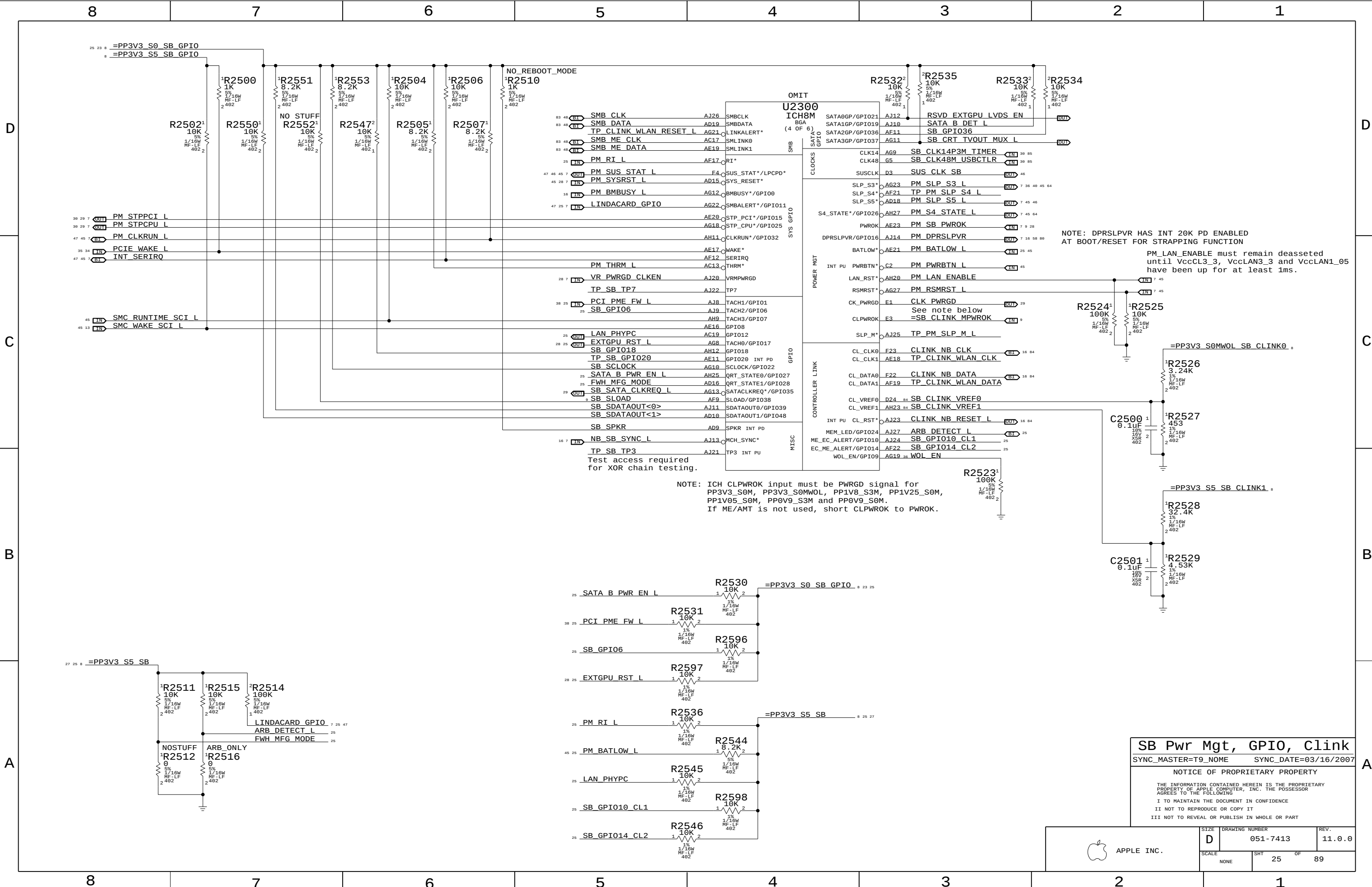
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB PCI, PCIe, DMI, USB		
SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007		
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NONE	24	89



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SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

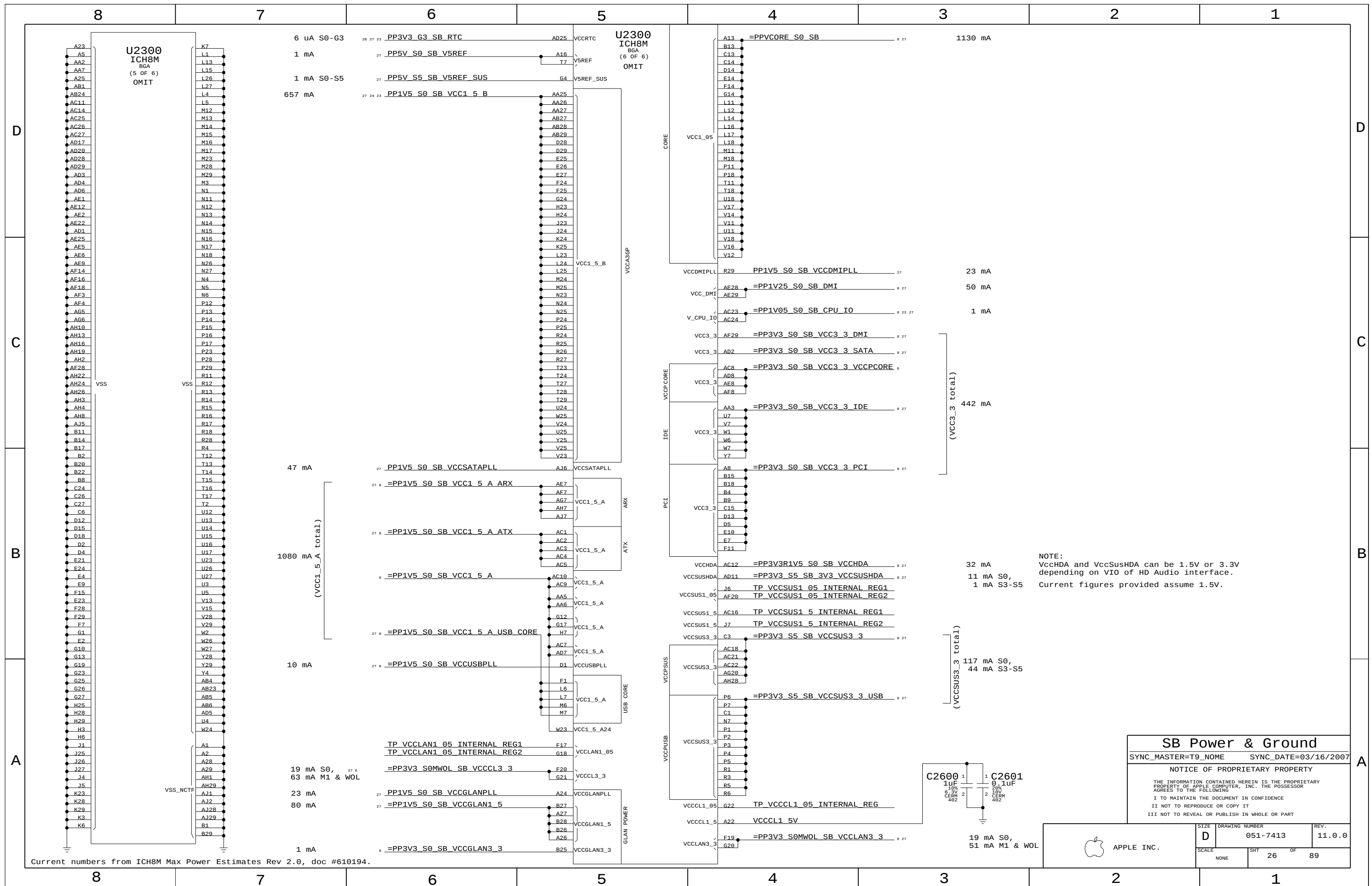
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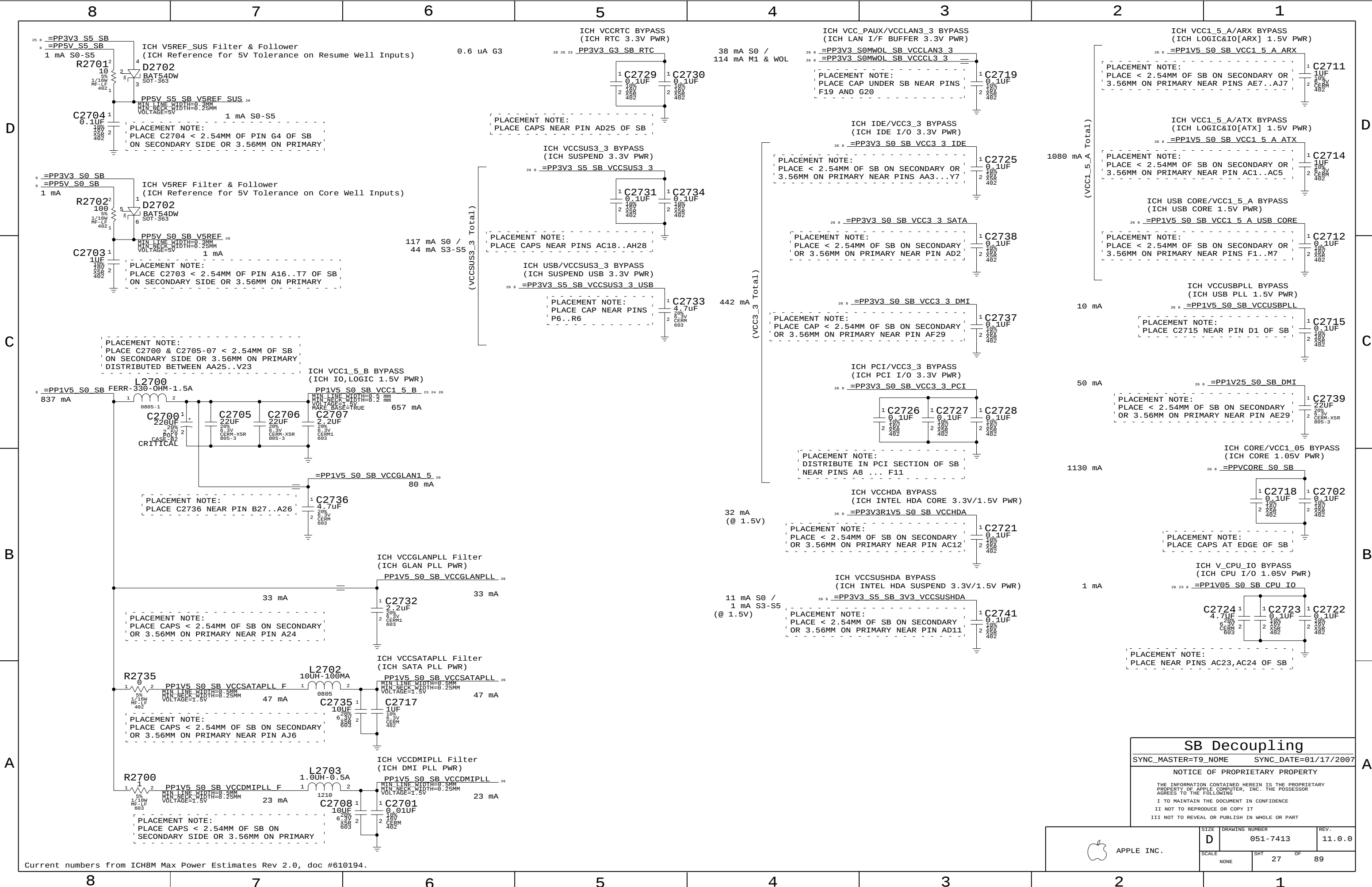
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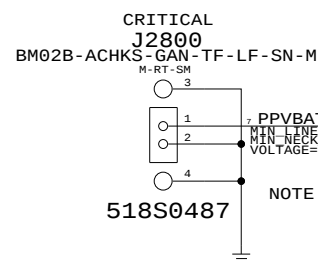
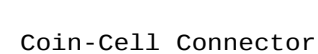


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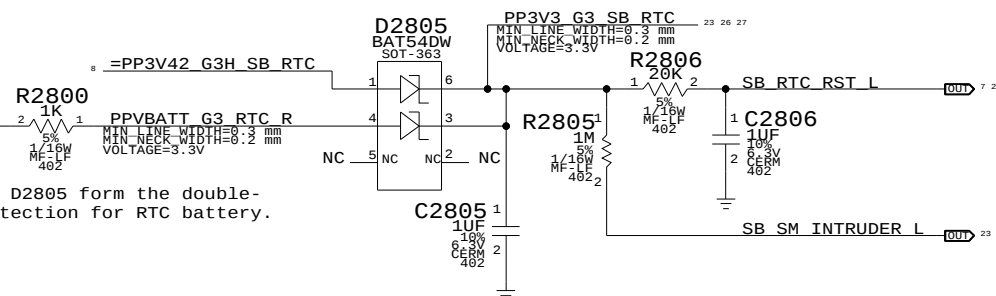
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SCALE	SHT	OF
NONE	25	89



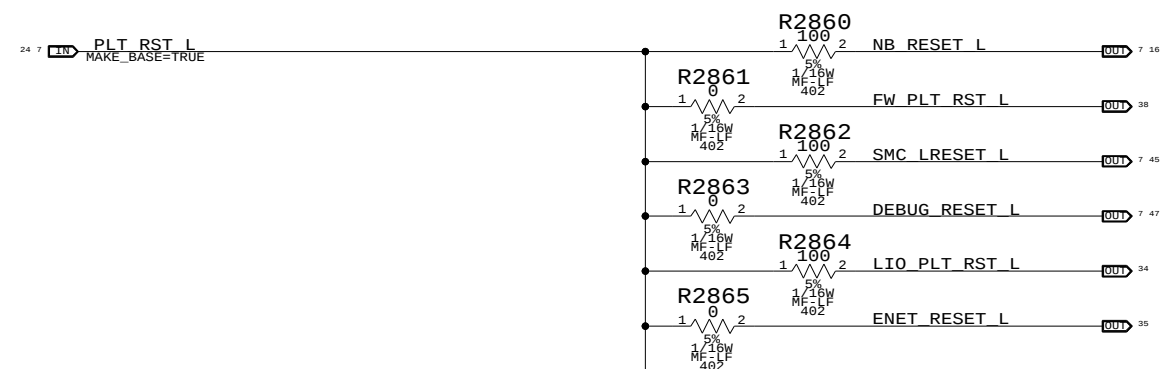




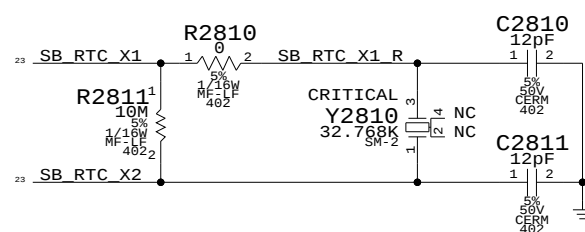
RTC Power Sources



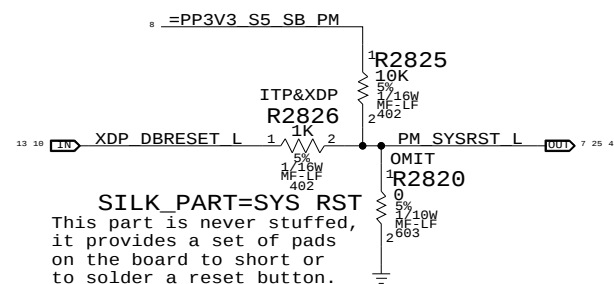
Platform Reset Connections



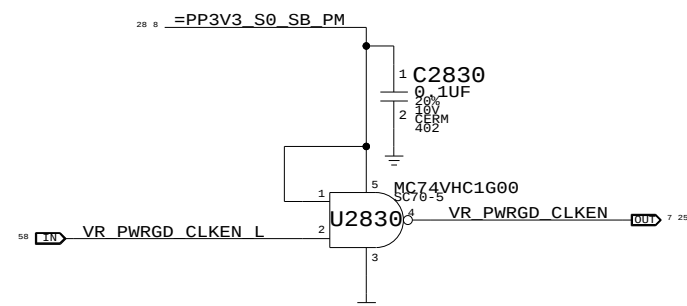
SB RTC Crystal



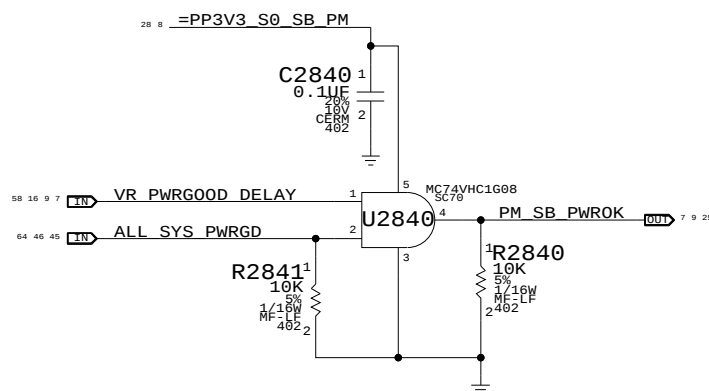
System Reset "Button"



VRMPWRGD Inverter



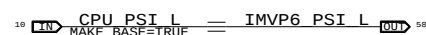
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI



SB Misc

SYNC_MASTER=(T9_MLB)	SYNC_DATE=08/24/2006
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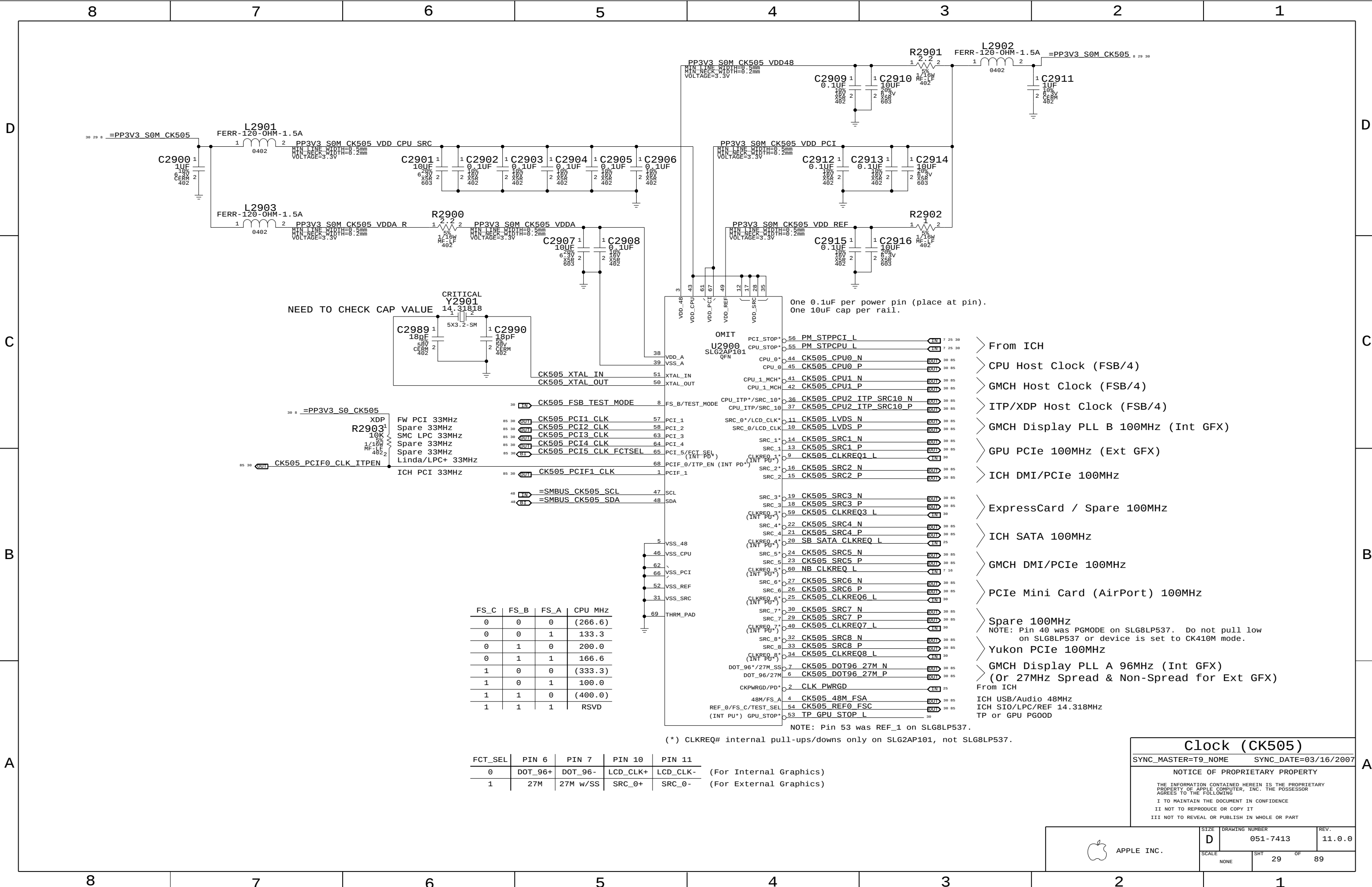
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SCALE	
	NO

SHT	
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89



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

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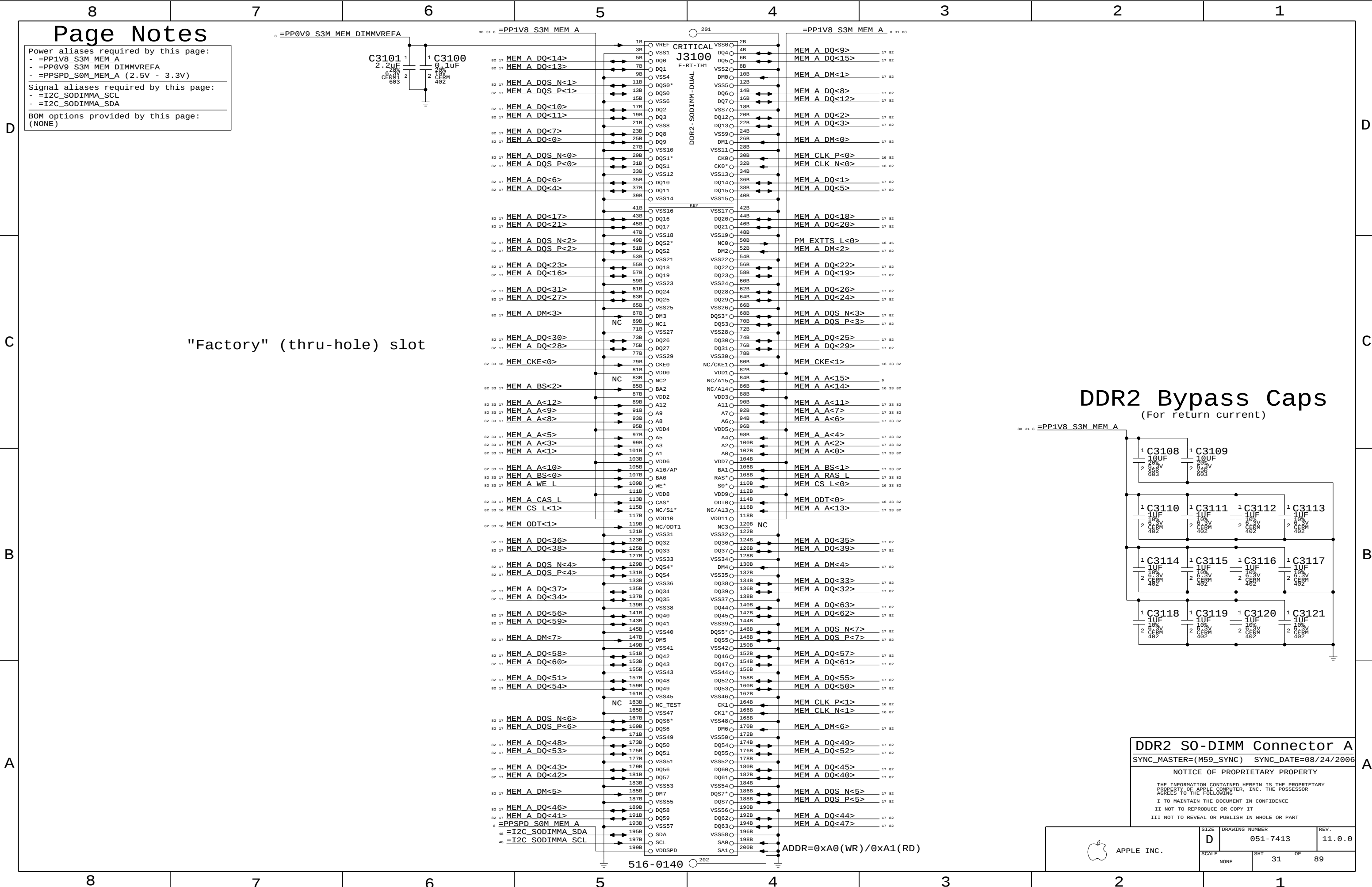
SIZE D

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REV. 11.0.0

SCALE NONE

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Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

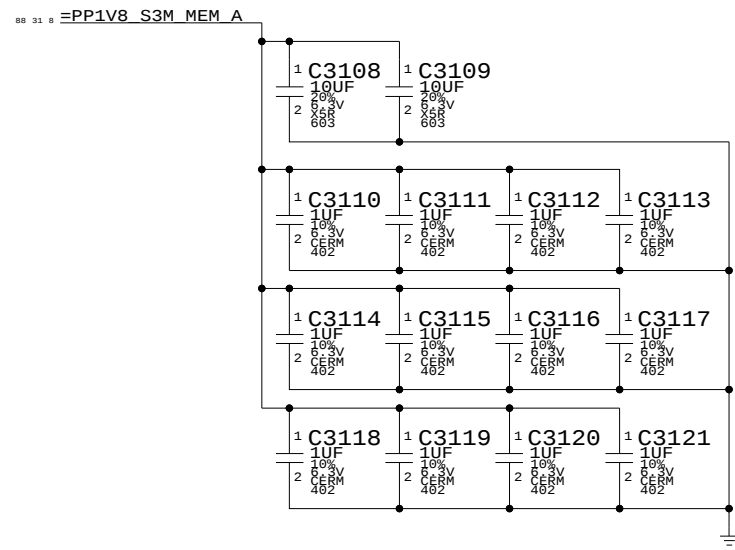
BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

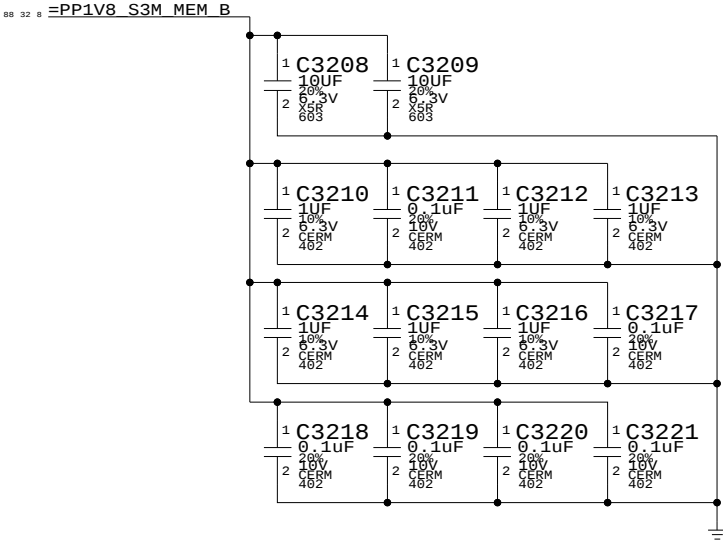
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SIZE

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SCALE

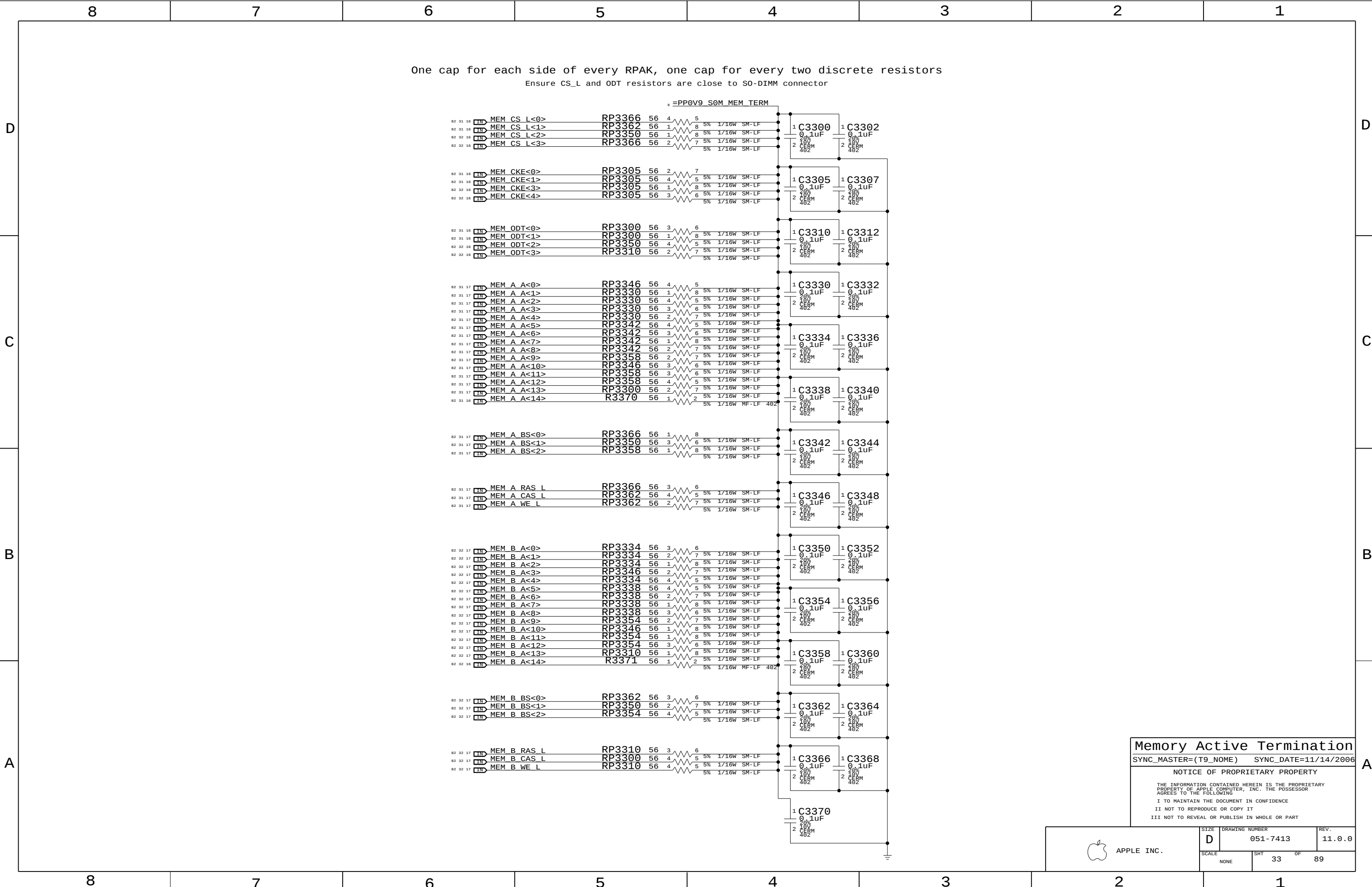
NONE

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Memory Active Termination

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SIZE

D

DRAWING NUMBER

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REV.

11.0.0

SCALE

NONE

SHT

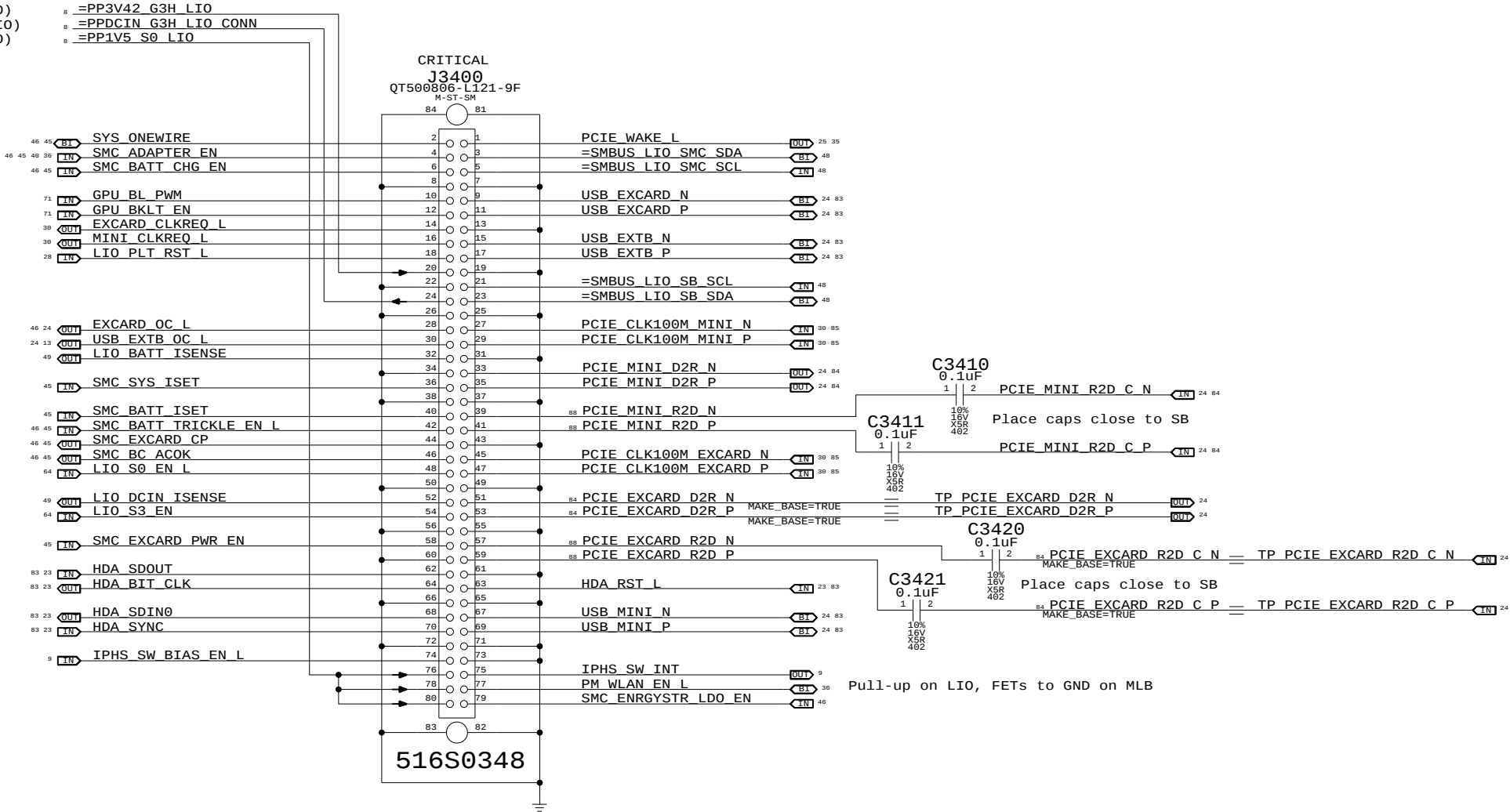
33

OF

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Left I/O Board Connector

(Output to LIO)
(Input from LIO)
(Output to LIO)



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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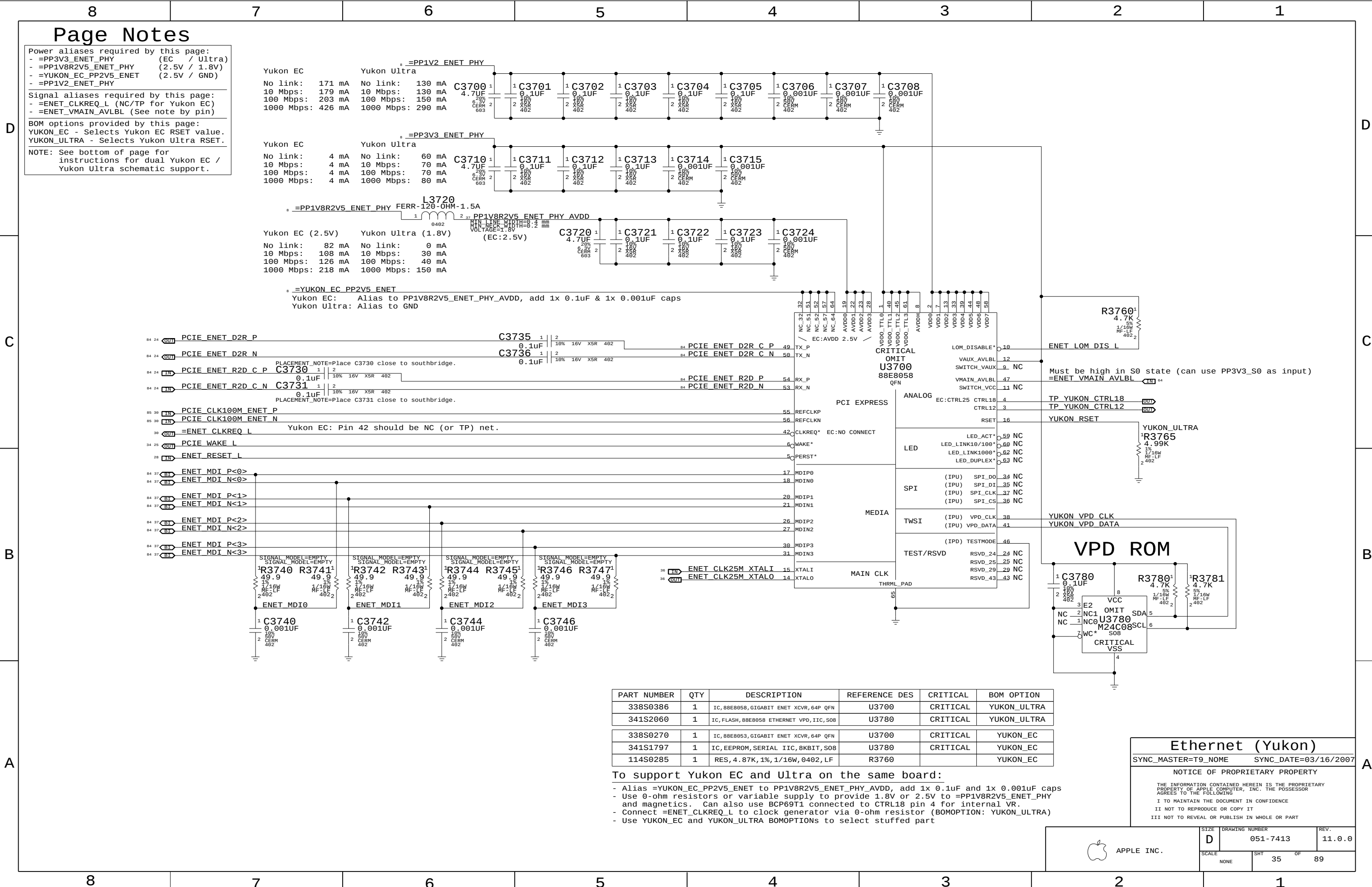
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SCALE	SHT	OF
NONE	34	89

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Page Notes

Power aliases required by this page:

- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:

- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

The schematic shows connections for PCIE ENET D2R P/N, PCIE ENET R2D C/P/N, PCIE CLK100M ENET P/N, =ENET_CLKREQ_L, PCIE WAKE L, ENET RESET L, ENET MDI P<0>/N<0>, ENET MDI P<1>/N<1>, ENET MDI P<2>/N<2>, ENET MDI P<3>/N<3>, ENET MDIO, ENET MDI1, ENET MDI2, ENET MDI3, ENET CLK25M XTALI/XTALO, ENET LOM DIS L, YUKON_CTRL18/CTRL12, YUKON_RSET, YUKON_VPD_CLK/VPD_DATA, VPD_ROM, and MAIN_CLK. Various passive components like capacitors (C3700-C3708, C3710-C3715, C3720-C3724, C3730-C3736, C3740-C3746, C3780), resistors (R3740-R3746, R3760, R3765, R3780, R3781), and ICs (U3700, U3780, M24C08) are shown with their values and footprints.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, 6GIGABIT ETHERNET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, 6GIGABIT ETHERNET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE NONE SHOT 35 OF 89

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

Schematic Diagram:

The diagram shows the electrical connections for the Ethernet (Yukon) interface. It includes power planes for PP1V2, PP3V3, and PP1V8R2V5, each with decoupling capacitors (C3700-C3708, C3710-C3715, C3720-C3724). Signal lines include PCIE ENET D2R P/N, PCIE ENET R2D C/P/N, ENET MDI P<0>/N<0>, ENET MDI P<1>/N<1>, ENET MDI P<2>/N<2>, ENET MDI P<3>/N<3>, ENET CLKREQ L, ENET RESET L, ENET MDIO, ENET MDI1, ENET MDI2, ENET MDI3, ENET CLK25M XTALI/XTALO, and MAIN CLK. The diagram also shows the connection to the VPD ROM (U3780) and the YUKON_CTRL18/YUKON_CTRL12 pins.

Table 1: Power Aliases

Alias	Value
=PP3V3_ENET_PHY	(EC / Ultra)
=PP1V8R2V5_ENET_PHY	(2.5V / 1.8V)
=YUKON_EC_PP2V5_ENET	(2.5V / GND)
=PP1V2_ENET_PHY	

Table 2: Signal Aliases

Alias	Description
=ENET_CLKREQ_L	(NC/TP for Yukon EC)
=ENET_VMAIN_AVLBL	(See note by pin)

Table 3: BOM Options

Option	Description
YUKON_EC	Selects Yukon EC RSET value.
YUKON_ULTRA	Selects Yukon Ultra RSET.

Table 4: Component Values

Component	Value
C3700-C3708	0.1uF
C3710-C3715	0.1uF
C3720-C3724	0.1uF
R3760	4.7K
R3765	4.99K
R3780	4.7K
R3781	4.7K

Table 5: Part Numbers

Part Number	Qty	Description	Reference Des	Critical	BOM Option
338S0386	1	IC, 88E8058, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE NONE SHOT 35 OF 89

- This diagram illustrates the hardware configuration for Ethernet (Yukon) on a board, showing various components, their connections, and associated BOM options.

Page Notes

Power aliases required by this page:

 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

Signal aliases required by this page:

 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:

YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

Schematic Details

The schematic shows the connection of various components to the board's pins and internal signals.

 - Power Aliases:** =PP1V2_ENET_PHY, =PP3V3_ENET_PHY, =PP1V8R2V5_ENET_PHY, =YUKON_EC_PP2V5_ENET.
 - Capacitors:** C3700-C3708, C3710-C3715, C3720-C3724, C3730-C3736, C3740-C3746, C3780, C3781.
 - Resistors:** R3740-R3746, R3760, R3765, R3780.
 - Inductors:** L3720.
 - ICs:** U3700 (88E8058 QFN), U3780 (M24C08 SCL).
 - Connectors:** ENET MDI P<0>, ENET MDI N<0>, ENET MDI P<1>, ENET MDI N<1>, ENET MDI P<2>, ENET MDI N<2>, ENET MDI P<3>, ENET MDI N<3>.
 - Other Components:** LOM_DISABLE*, VAUX_AVLBL, SWITCH_VAUX, VMAIN_AVLBL, SWITCH_VCC, CTRL18, CTRL12, RSET, LED_ACT*, LED_LINK1000*, LED_LINK1000*, LED_DUPLEX*, SPI_DO, SPI_DI, SPI_CLK, SPI_CS, VPD_CLK, VPD_DATA, TESTMODE, RSVD_24, RSVD_25, RSVD_29, RSVD_43.

BOM Options

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

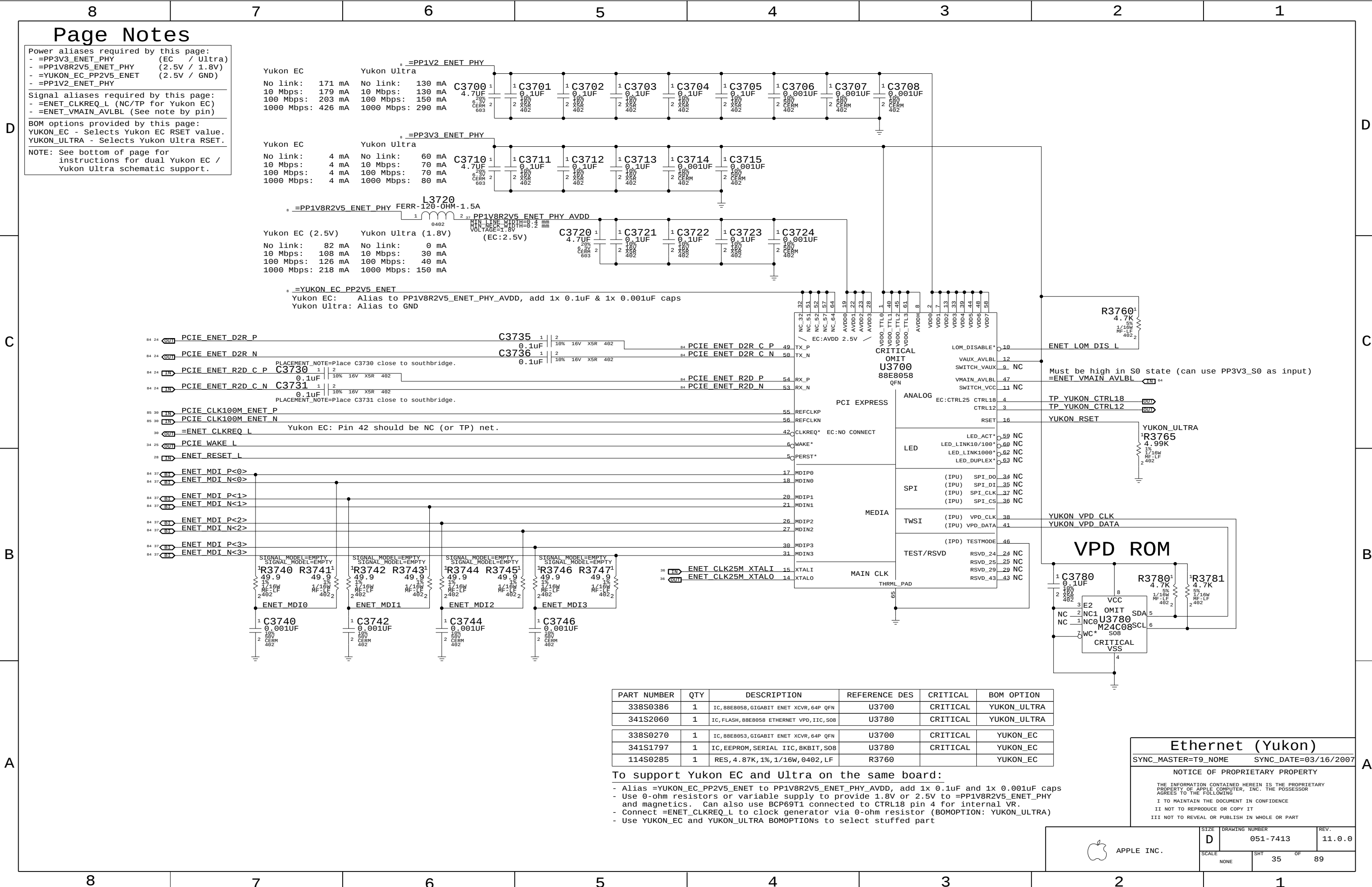
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SCALE NONE SHOT 35 OF 89

[illegible]

This diagram illustrates the hardware configuration for Ethernet (Yukon) on a board, showing various components, their connections, and associated BOM options.

Page Notes:

- Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY
- Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBL (See note by pin)
- BOM options provided by this page:
 - YUKON_EC - Selects Yukon EC RSET value.
 - YUKON_ULTRA - Selects Yukon Ultra RSET.
- NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

Component Details and Connections:

- Capacitors:** C3700-C3708, C3710-C3715, C3720-C3724, C3730-C3736, C3740-C3746, C3780, C3781, C3782.
- Resistors:** R3740-R3746, R3760, R3765, R3780, R3781, R3782.
- Inductors:** L3720.
- ICs:** U3700 (88E8058 QFN), U3780 (M24C08 SCL), U3781 (M24C08 SCL).
- Connectors:** ENET MDI P<0>, ENET MDI N<0>, ENET MDI P<1>, ENET MDI N<1>, ENET MDI P<2>, ENET MDI N<2>, ENET MDI P<3>, ENET MDI N<3>.
- Other Components:** LOM_DISABLE*, VAUX_AVLBL, SWITCH_VAUX, VMAIN_AVLBL, SWITCH_VCC, CTRL18, CTRL12, RSET, LED_ACT*, LED_LINK1000*, LED_LINK1000*, LED_DUPLEX*, YUKON_CTRL18, YUKON_CTRL12, YUKON_RSET, YUKON_ULTRA, YUKON_VPD_CLK, YUKON_VPD_DATA, VPD ROM.

Table 1: Part Numbers and Quantities

PART NUMBER	QTY
338S0386	1
341S2060	1
338S0270	1
341S1797	1
114S0285	1

Table 2: Description and Reference Designators

DESCRIPTION	REFERENCE DES
IC, 88E8058, 64P QFN	U3700
IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780
IC, 88E8053, 64P QFN	U3700
IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780
RES, 4.87K, 1%, 1/16W, 0402, LF	R3760

Table 3: Criticality and BOM Options

Criticality	BOM OPTION
CRITICAL	YUKON_ULTRA
CRITICAL	YUKON_ULTRA
CRITICAL	YUKON_EC
CRITICAL	YUKON_EC
	YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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[illegible]

D

C

B



CRITICAL

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

1.9V for Yukon Ultra, 2.5V for Yukon EC

D

C

B

8

7



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D	051-7413	11.0.0

8

4

3

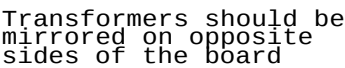
2

1

```
Power aliases required by this page:
- =GND_CHASSIS_ENET
```

```
Signal aliases required by this page:
(NONE)
```

```
BOM options provided by this page:
(NONE)
```



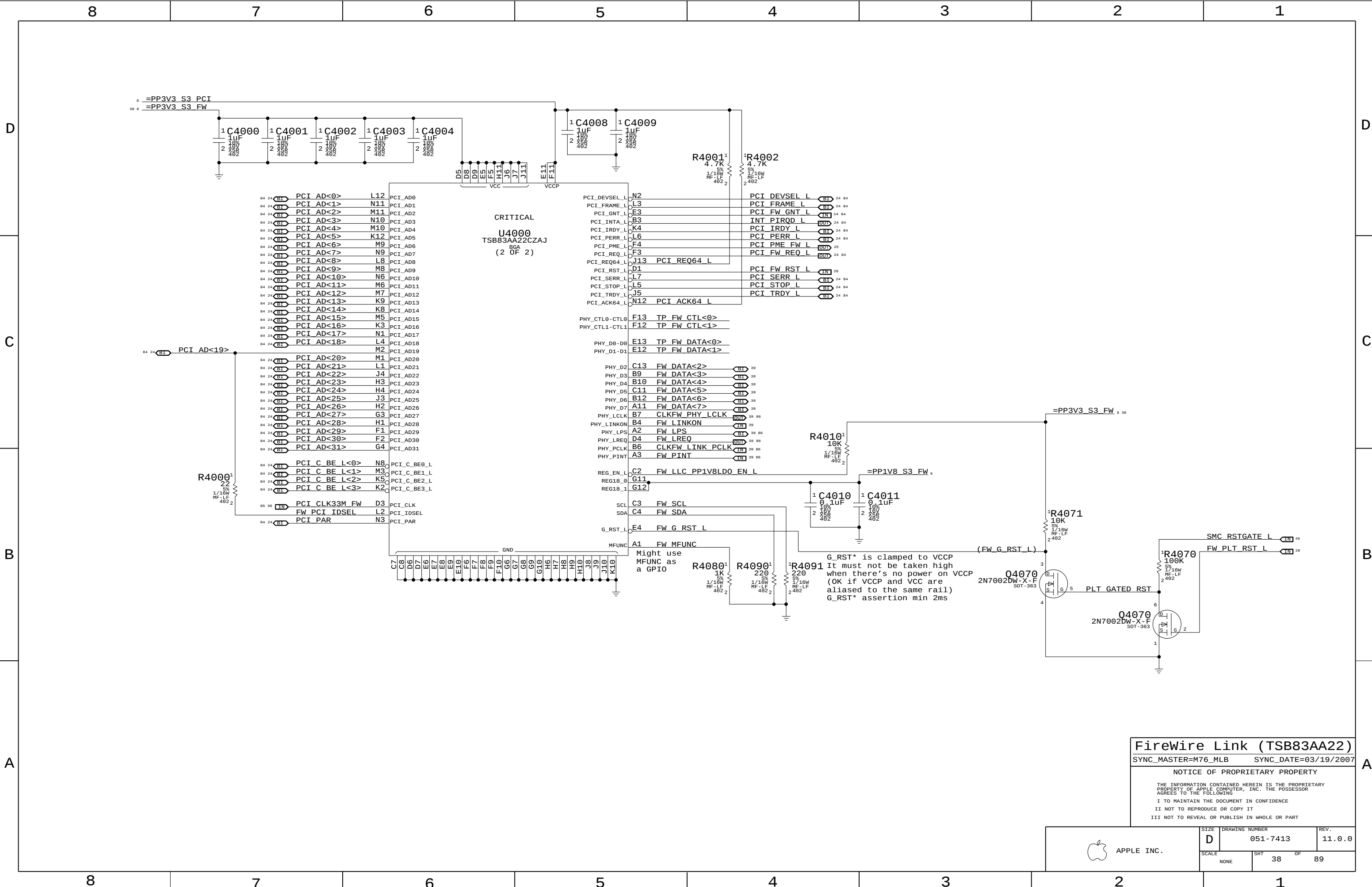
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0053	2	XFMR, ISO, HALF-PORT, 1000T, 16P, SMD, 2MM	T3900, T3901	CRITICAL	

Ethernet Connector	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

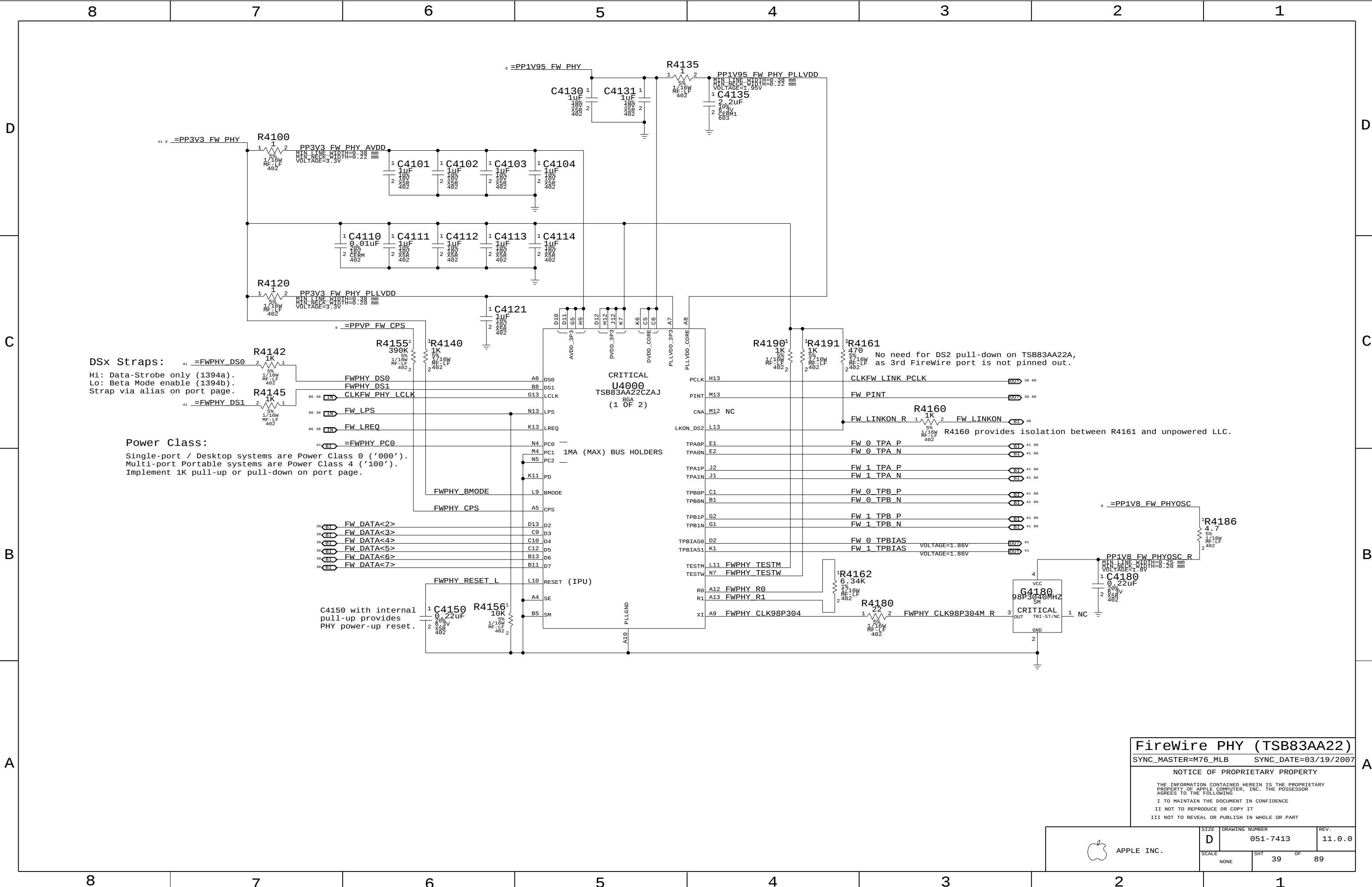
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SIZE	DRAWING NUMBER	REV.
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NONE	38	89



FireWire PHY (TSB83AA22)

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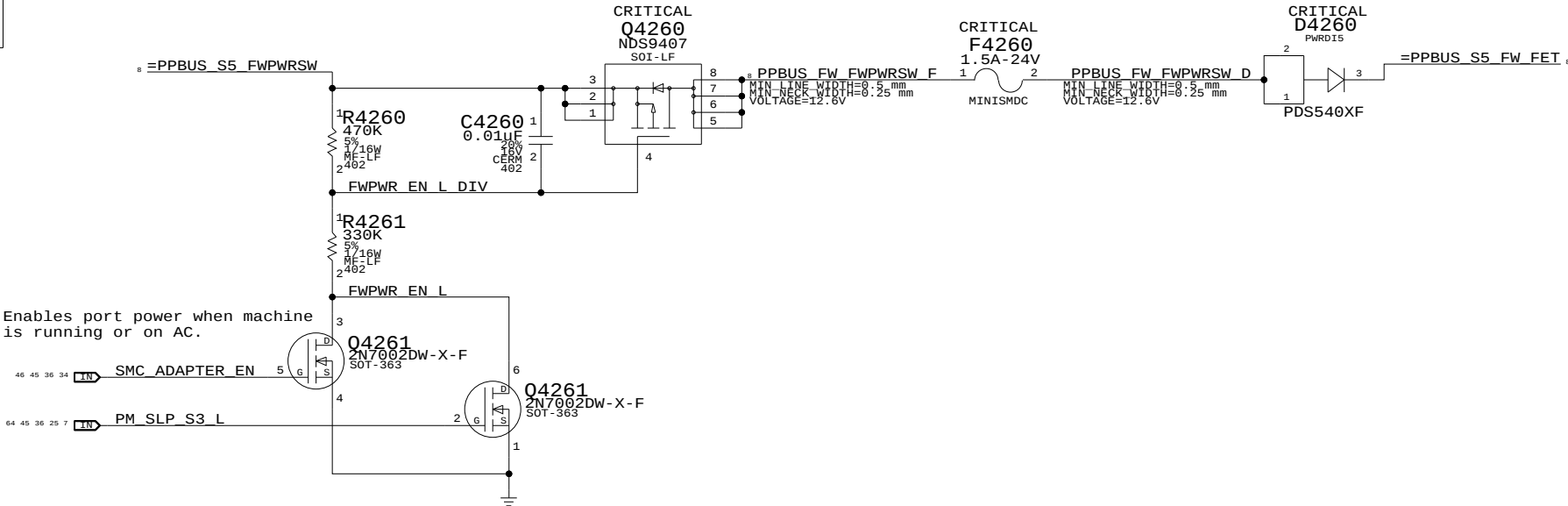
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	39	89

Page Notes

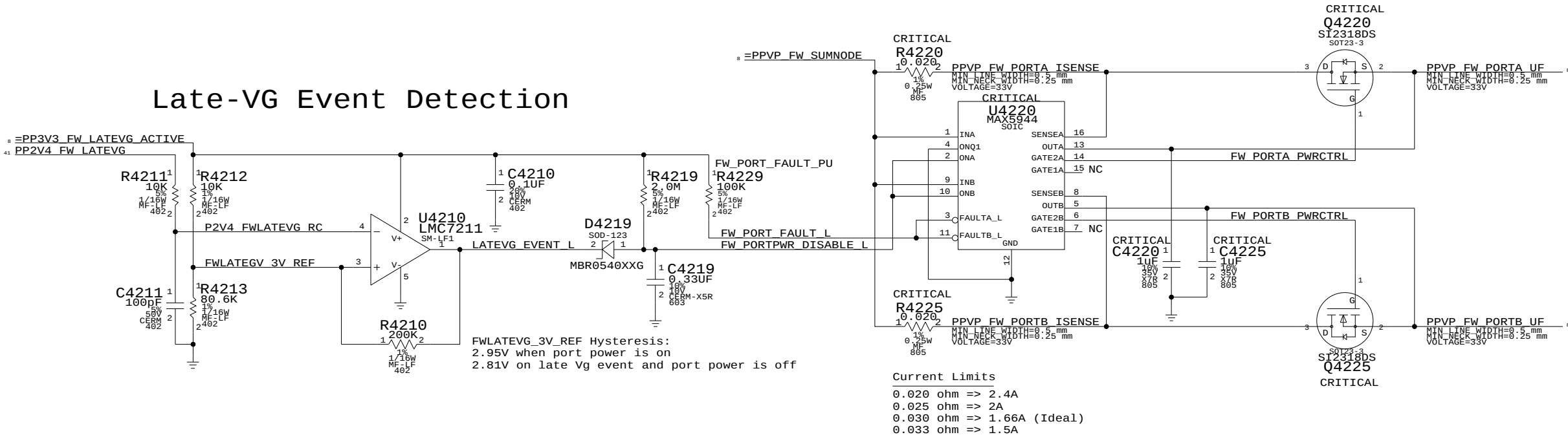
Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	40	89

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39

=PP3V3_FW_PHY

=FWPHY_PC0

=FWPHY_DS0

=FWPHY_DS1

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39

FW_1_TPBias

C4350

1uF

10%V

CE8M

402

C4360

1uF

10%V

CE8M

402

86

39

FW_0_TPA_P

R4350

56.2

1%V

MF-LF

402

R4351

56.2

1%V

MF-LF

402

86

39

FW_0_TPA_N

R4360

56.2

1%V

MF-LF

402

R4361

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_P

R4352

56.2

1%V

MF-LF

402

R4353

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_N

R4362

56.2

1%V

MF-LF

402

R4363

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_P

R4354

56.2

1%V

MF-LF

402

R4355

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_N

R4364

56.2

1%V

MF-LF

402

R4365

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_P

R4356

56.2

1%V

MF-LF

402

R4357

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_N

R4366

56.2

1%V

MF-LF

402

R4367

56.2

1%V

MF-LF

402

86

39

FW_0_TPA_P

C4350

1uF

10%V

CE8M

402

C4360

1uF

10%V

CE8M

402

86

39

FW_0_TPA_N

R4350

56.2

1%V

MF-LF

402

R4351

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_P

R4352

56.2

1%V

MF-LF

402

R4353

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_N

R4362

56.2

1%V

MF-LF

402

R4363

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_P

R4354

56.2

1%V

MF-LF

402

R4355

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_N

R4364

56.2

1%V

MF-LF

402

R4365

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_P

R4356

56.2

1%V

MF-LF

402

R4357

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_N

R4366

56.2

1%V

MF-LF

402

R4367

56.2

1%V

MF-LF

402

86

39

FW_0_TPA_P

C4350

1uF

10%V

CE8M

402

C4360

1uF

10%V

CE8M

402

86

39

FW_0_TPA_N

R4350

56.2

1%V

MF-LF

402

R4351

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_P

R4352

56.2

1%V

MF-LF

402

R4353

56.2

1%V

MF-LF

402

86

39

FW_0_TPB_N

R4362

56.2

1%V

MF-LF

402

R4363

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_P

R4354

56.2

1%V

MF-LF

402

R4355

56.2

1%V

MF-LF

402

86

39

FW_1_TPA_N

R4364

56.2

1%V

MF-LF

402

R4365

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_P

R4356

56.2

1%V

MF-LF

402

R4357

56.2

1%V

MF-LF

402

86

39

FW_1_TPB_N

R4366

56.2

1%V

MF-LF

402

R4367

56.2

1%V

MF-LF

402

86

39

FW_0_TPA_P

C4350

1uF

10%V

CE8M

40

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

39 # =PP3V3 FW PHY

39 # =FWPHY PC0

39 # =FWPHY DS0

39 # =FWPHY DS1

TI PHYs require 1uF even though FW spec calls out 0.33uF

FW 1 TPBIAS
FW 0 TPBIAS

1 C4350 1uF 10% 6.3V CERM 402
2

1 C4360 1uF 10% 6.3V CERM 402
2

CRITICAL L4360 18NH-250MA
0402
FW B TPA L P

CRITICAL L4361 18NH-250MA
0402
FW B TPA L N

1 R4350 56.2 1% 1/16W NF-L 402
2

1 R4351 56.2 1% 1/16W NF-L 402
2

1 R4360 56.2 1% 1/16W NF-L 402
2

1 R4361 56.2 1% 1/16W NF-L 402
2

FW 0 TPA P
FW 0 TPA N
FW 0 TPB P
FW 0 TPB N
FW 1 TPA P
FW 1 TPA N
FW 1 TPB P
FW 1 TPB N

FW PORT0 TPA P
MAKE_BASE=TRUE
FW PORT0 TPA N
MAKE_BASE=TRUE
FW PORT0 TPB P
MAKE_BASE=TRUE
FW PORT0 TPB N
MAKE_BASE=TRUE
FW PORT1 TPA P
MAKE_BASE=TRUE
FW PORT1 TPA N
MAKE_BASE=TRUE
FW PORT1 TPB P
MAKE_BASE=TRUE
FW PORT1 TPB N
MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY
1 R4352 56.2 1% 1/16W NF-L 402
2

1 R4353 56.2 1% 1/16W NF-L 402
2

1 R4362 56.2 1% 1/16W NF-L 402
2

1 R4363 56.2 1% 1/16W NF-L 402
2

FW B TPB L N
FW B TPB L P

CRITICAL L4362 18NH-250MA
0402
SIGNAL_MODEL=EMPTY
FW PORT1 TPB C

CRITICAL L4363 18NH-250MA
0402
SIGNAL_MODEL=EMPTY

FW PORT0 TPB C

1 C4354 220pF 5% 2 CERM 402
2

1 R4354 4.99K 1% 1/16W NF-L 402
2

1 C4364 220pF 5% 2 CERM 402
2

1 R4364 4.99K 1% 1/16W NF-L 402
2

LATEVG needs to be biased
 at 2.1V for FW signal integrity
 be biased to 2.4V for margin
 should be 390 Ohms max for a 3.3V rail

"Snapback" & "Late VG" Protection

PP2V4_FW_LATEVG

PPVP_FW_PORT1

FW_PORT1_TP* N

FW_PORT1_TP* P

FW_PORT1_TPA N

FW_PORT1_TPA P

DP4310 BAV99DW-X-F

DP4311 BAV99DW-X-F

C4310 0.01uF

C4311 0.01uF

C4312 0.01uF

C4313 0.01uF

C4314 0.01uF

C4319 0.01uF

C4319 1M 5% 16W

514S0133

TPB<R> OUTPUT

TPB+ VP

TPA<R> INPUT

TPA+ TPA-

VG NC

BREF

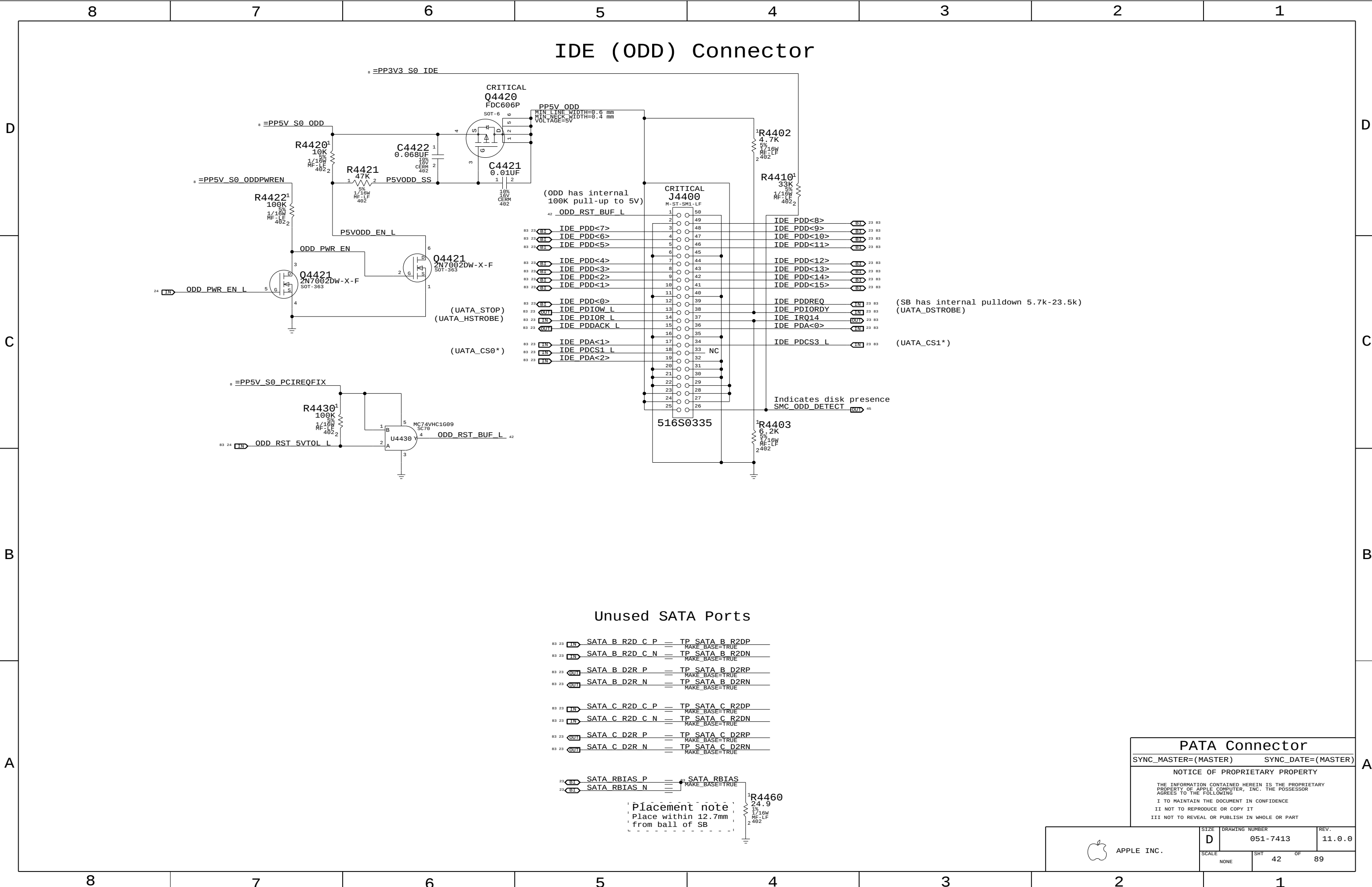
AREF

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

29



IDE (ODD) Connector

Unused SATA Ports

- SATA B R2D C P == TP SATA B R2DP
- SATA B R2D C N == TP SATA B R2DN
- SATA B D2R P == TP SATA B D2RP
- SATA B D2R N == TP SATA B D2RN
- SATA C R2D C P == TP SATA C R2DP
- SATA C R2D C N == TP SATA C R2DN
- SATA C D2R P == TP SATA C D2RP
- SATA C D2R N == TP SATA C D2RN

- SATA RBIAS P == SATA RBIAS
- SATA RBIAS N == MAKE_BASE=TRUE

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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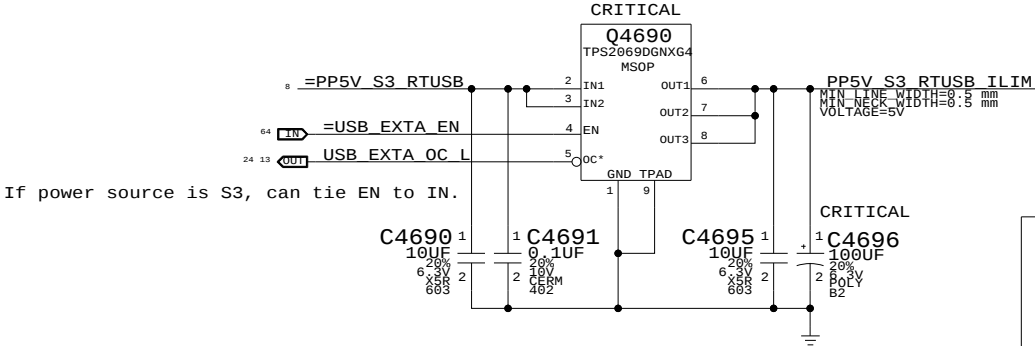
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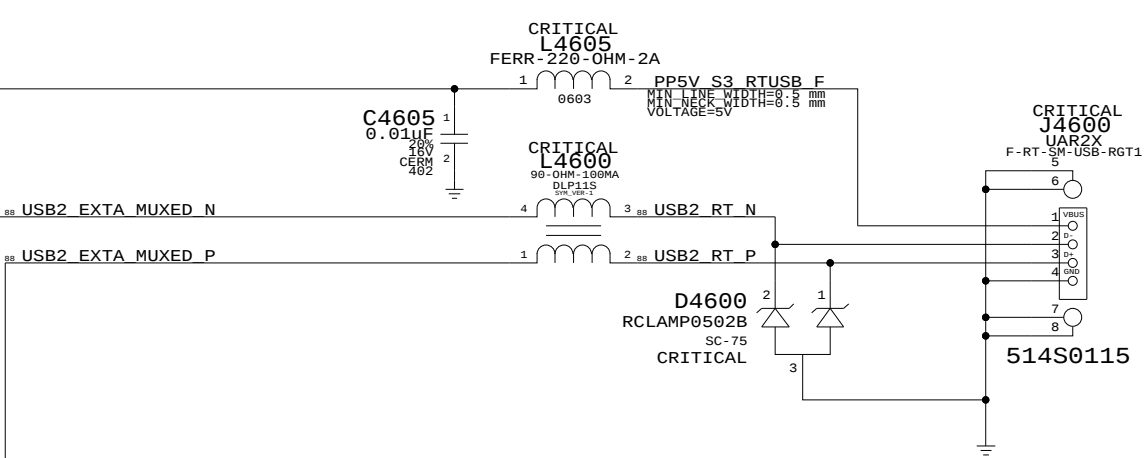
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	42	89

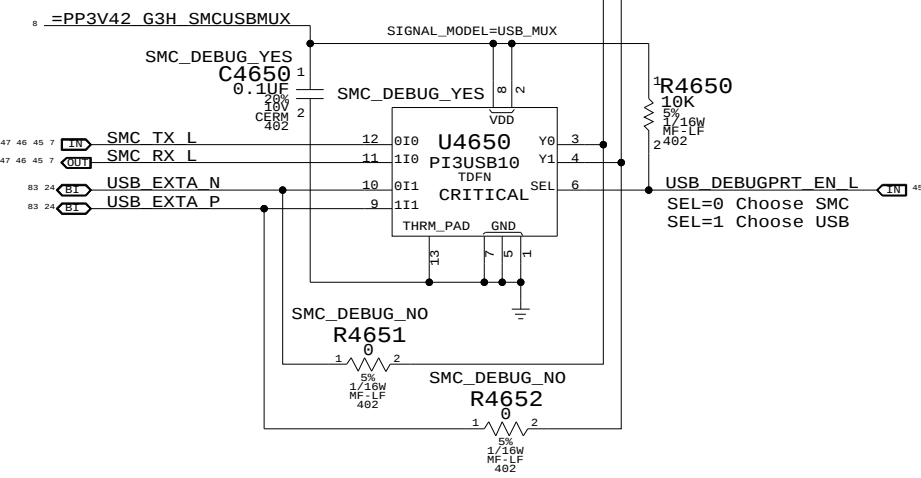
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

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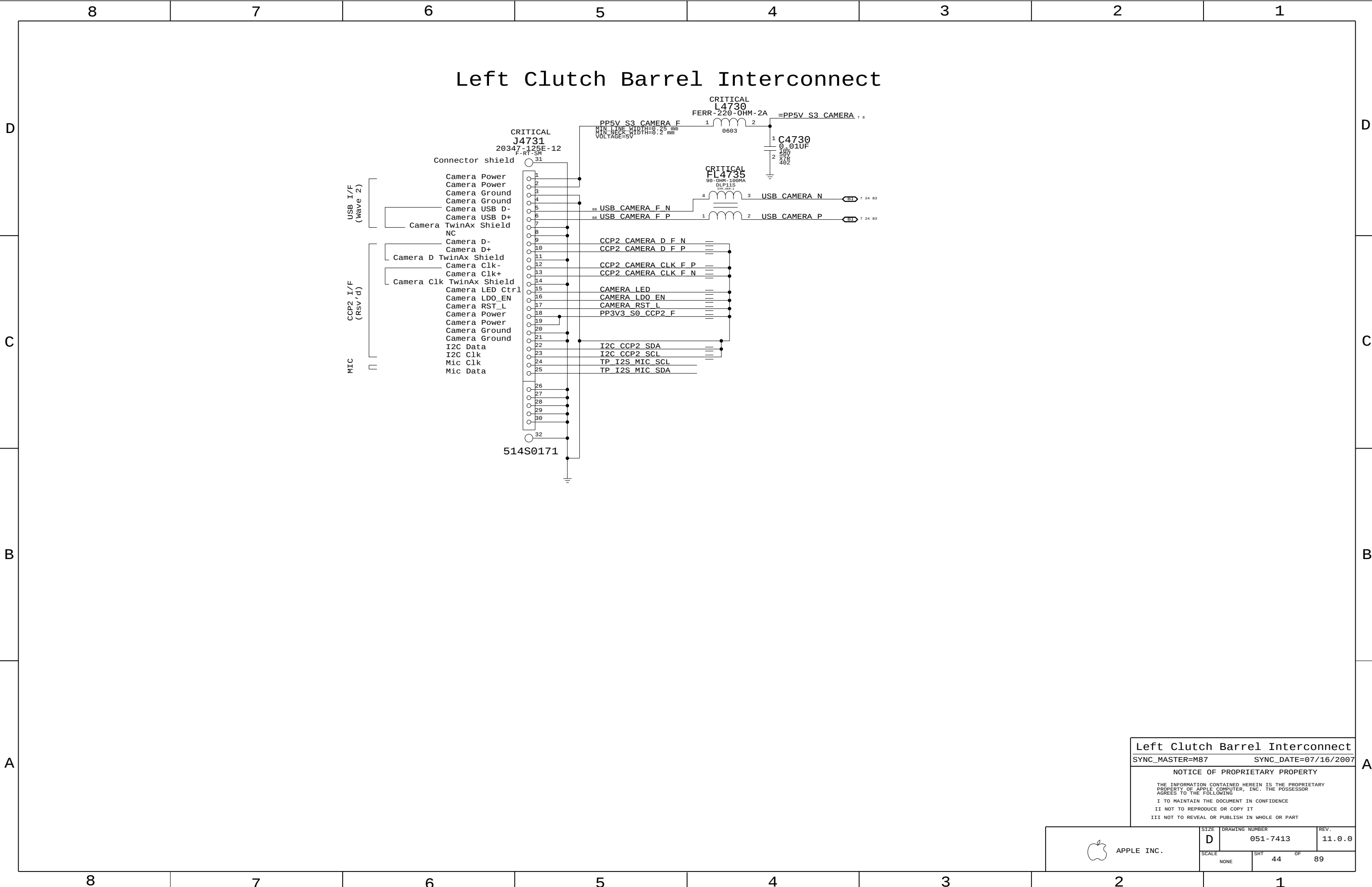
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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	43	89



Left Clutch Barrel Interconnect

SYNC_MASTER=M87

SYNC_DATE=07/16/2007

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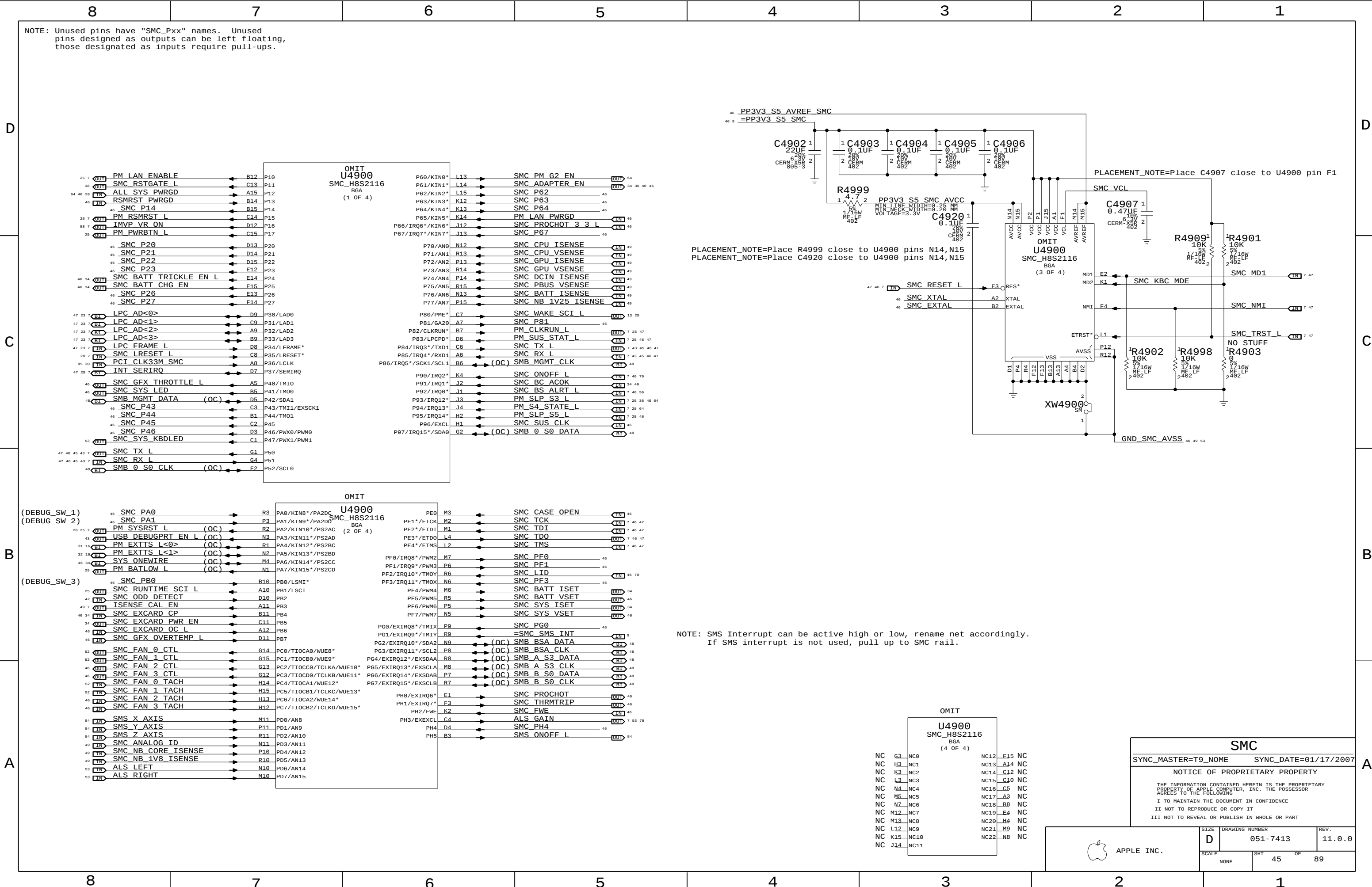
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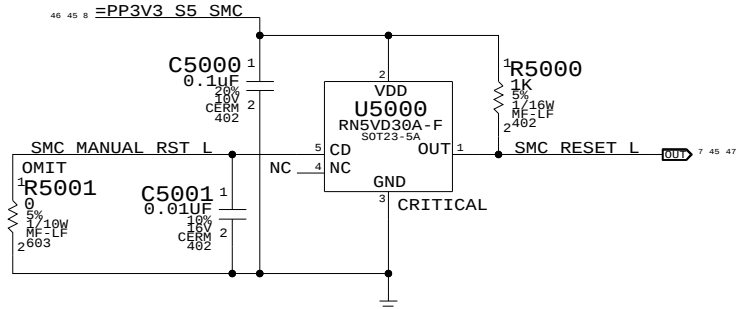
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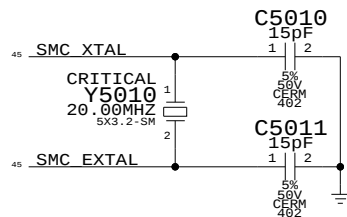
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 44	OF 89



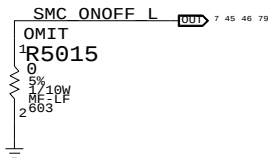
SMC Reset "Button" / Brownout Detect



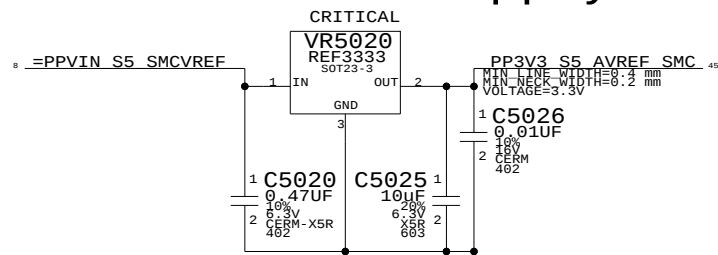
SMC Crystal Circuit



Debug Power "Button"

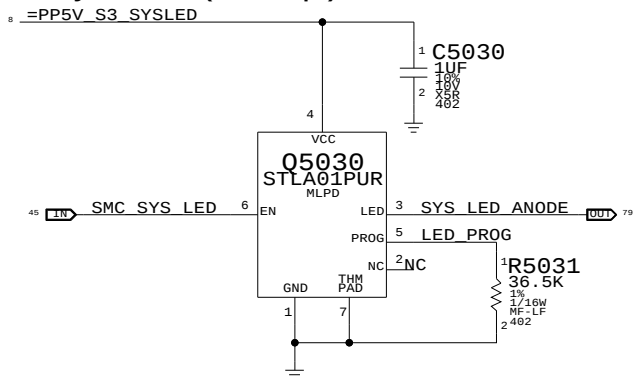


SMC AVREF Supply

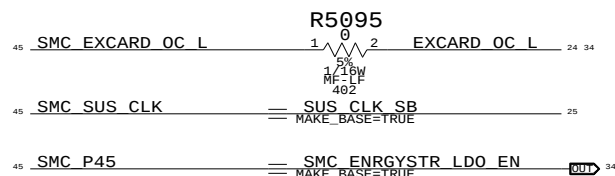
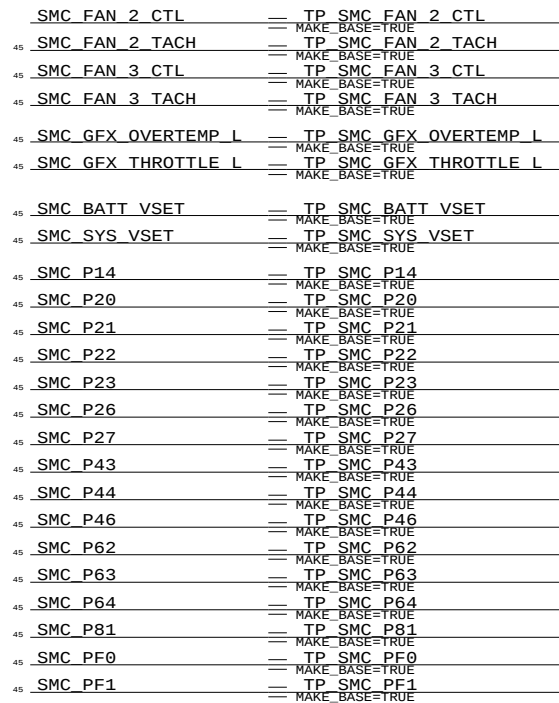
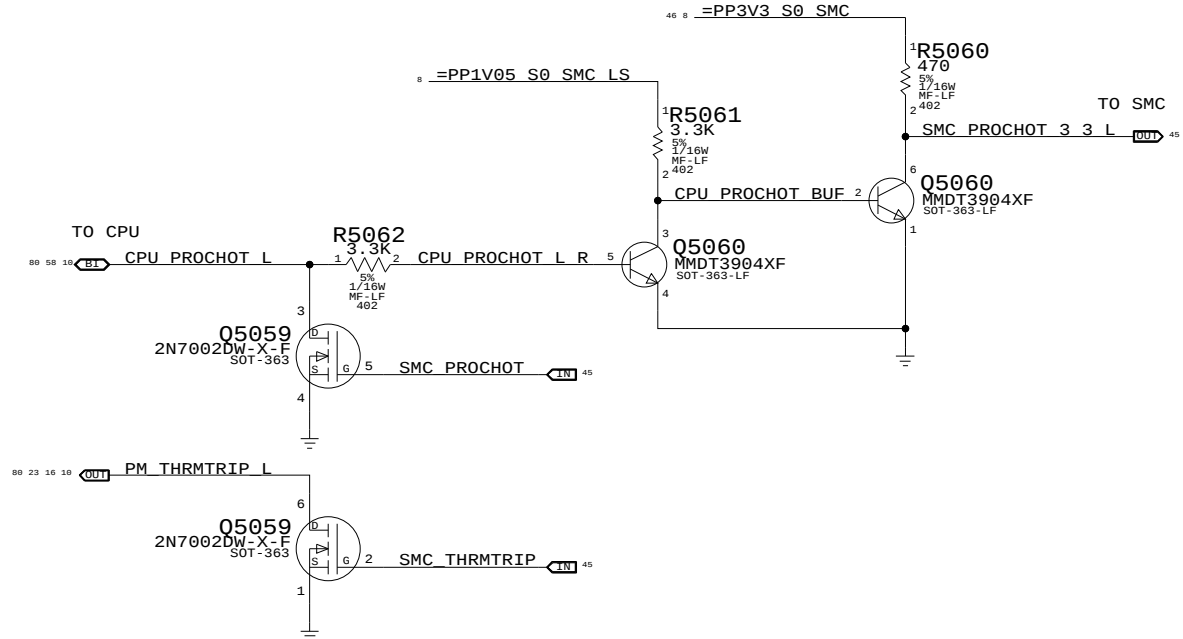


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

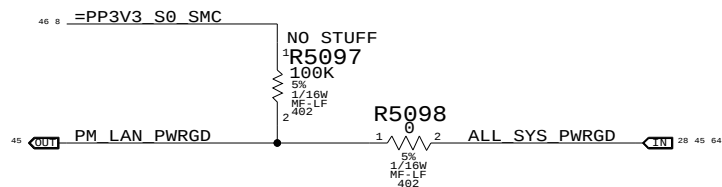
System (Sleep) LED Circuit



SMC FSB to 3.3V Level Shifting

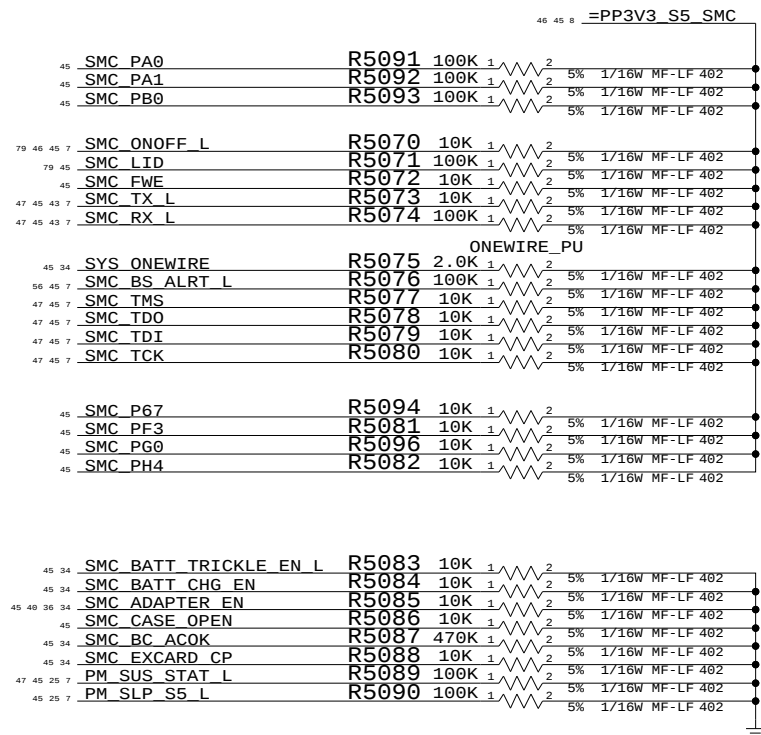
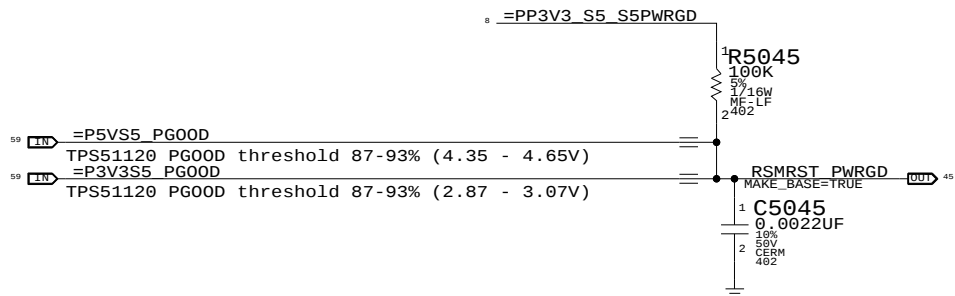


LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC Support

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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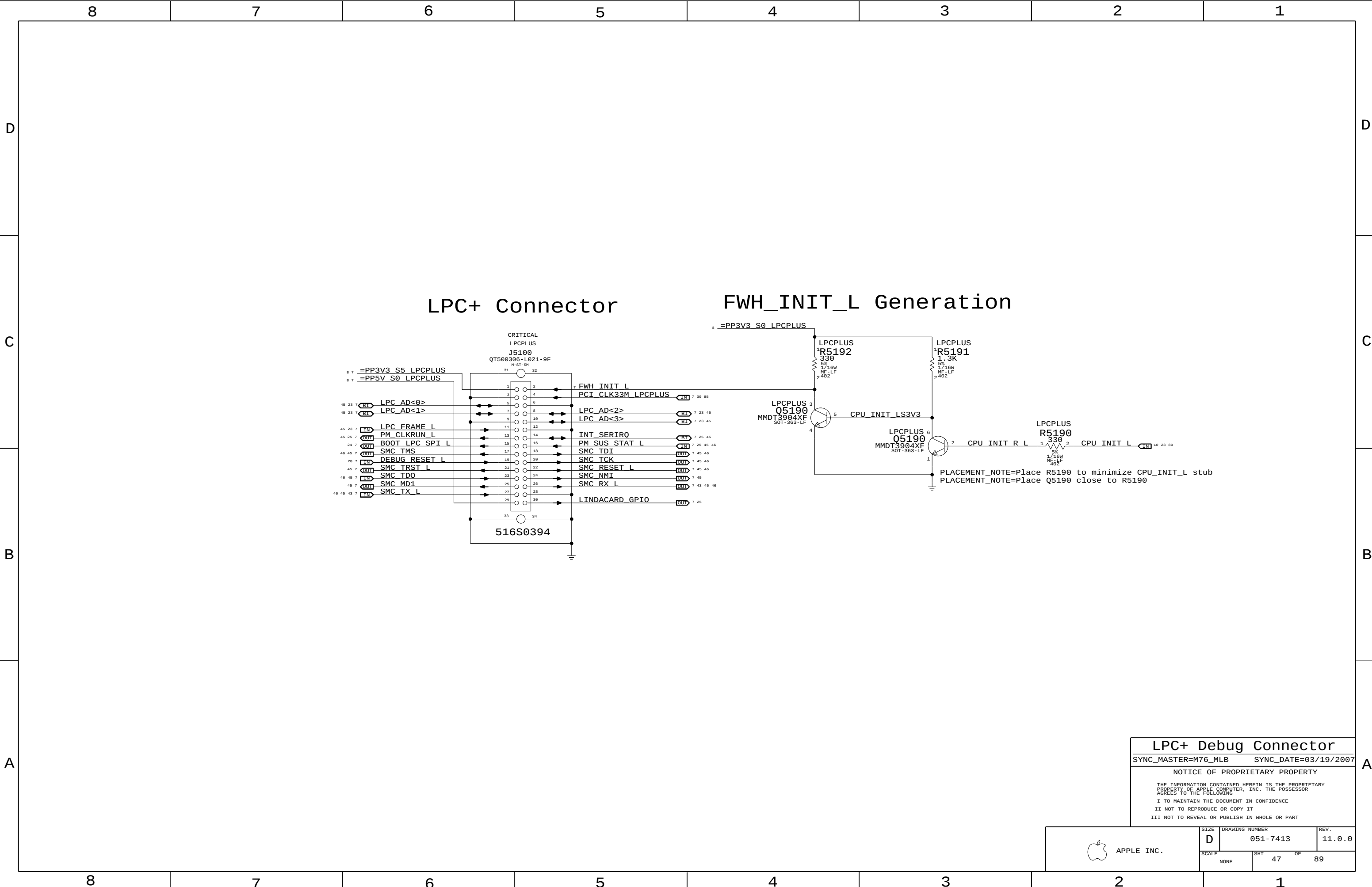
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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	46	89

 APPLE INC.



LPC+ Debug Connector

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007

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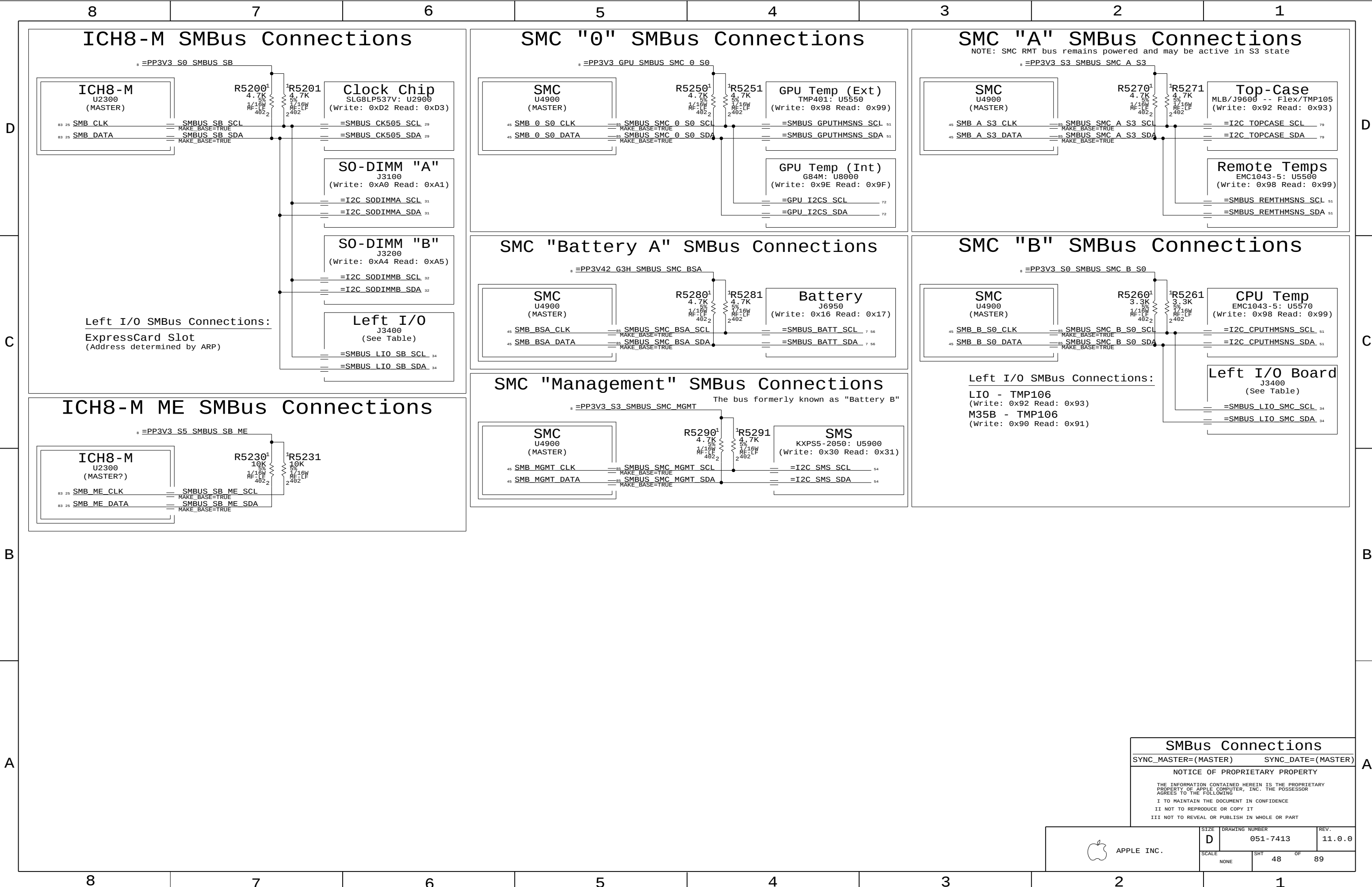
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 47	OF 89



SMBus Connections

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

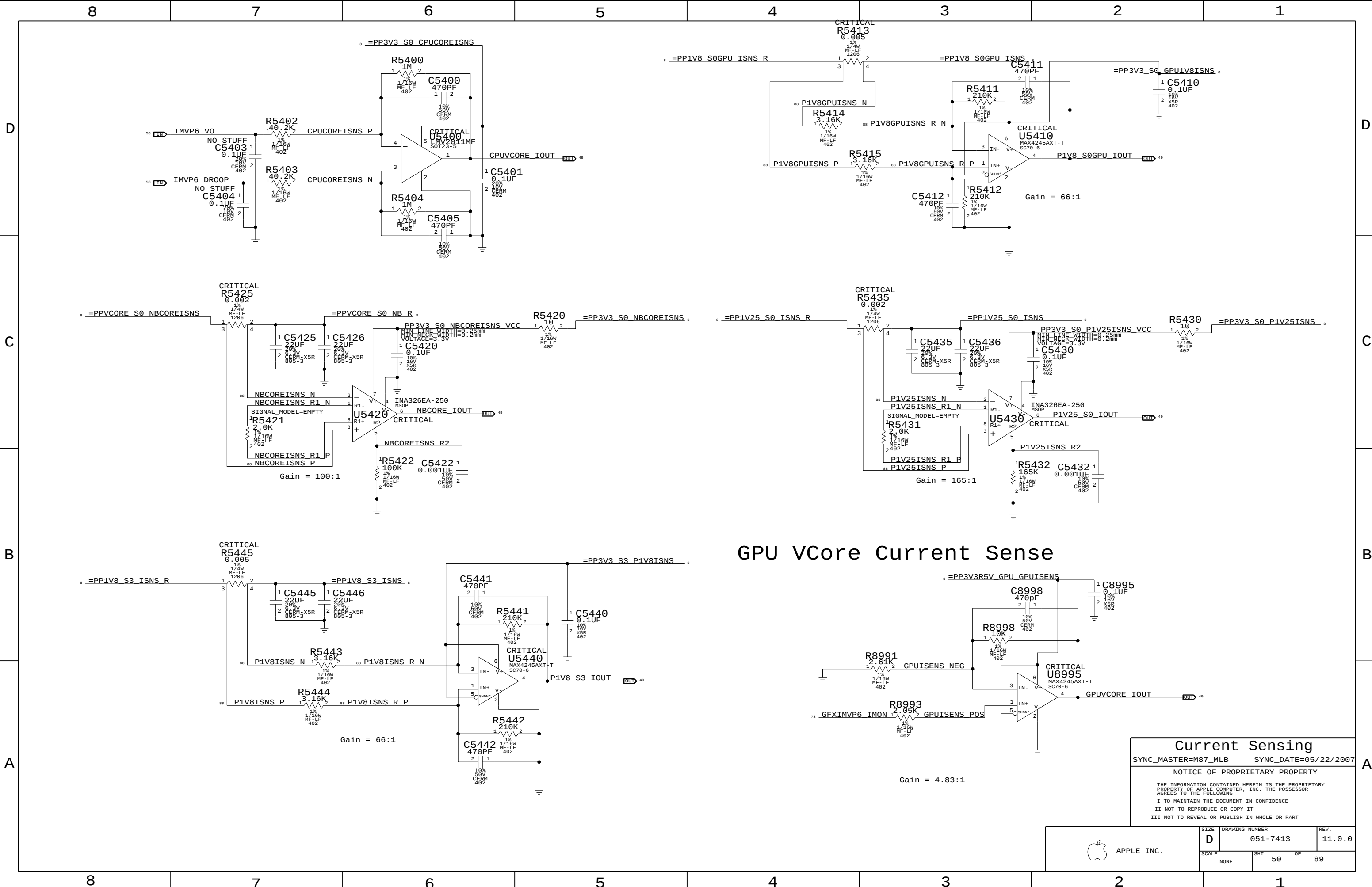
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GPU VCore Current Sense

Current Sensing

SYNC_MASTER=M87_MLB SYNC_DATE=05/22/2007

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	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		50	89

The schematic diagram illustrates the electrical connections for the CPU module, including the CPU, CPU thermistor, and CPU fan. The CPU is an EMC1403-1-AIZL (U5570) with a TSSOP package. The CPU thermistor is a C5580 (470PF) with a 10K resistance. The CPU fan is a J5590 (BM02B-ACHKS-GAN-TF-LF-SN-M) with a 10K resistance. The diagram shows the connection of the CPU to the CPU thermistor and the CPU fan, and the connection of the CPU thermistor to the CPU fan. The CPU is connected to the CPU thermistor via a 10K resistor (R5571) and a 10K resistor (R5572). The CPU is connected to the CPU fan via a 10K resistor (R5571) and a 10K resistor (R5572). The CPU is connected to the CPU thermistor via a 10K resistor (R5571) and a 10K resistor (R5572). The CPU is connected to the CPU fan via a 10K resistor (R5571) and a 10K resistor (R5572).

26	BI	=NB	TDB	FORCE	---
26	BI	=NB	TDB	SENSE	---
26	BI	=NB	TDE	SENSE	---
26	BI	=NB	TDE	FORCE	---

(Th1H)

CRITICAL
BM02B-ACHKS-GAN-TF-LF-SN-M
Place on left side of fan cutout

Placement note:
Place on left side of fan cutout

(TG0H)

CRITICAL
BM02B-ACHKS-GAN-TF-LF-SN-M
Place near GPU

Placement note:
Place near GPU

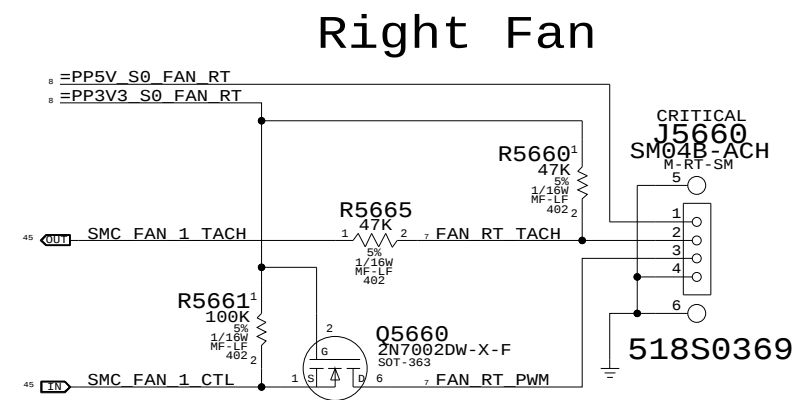
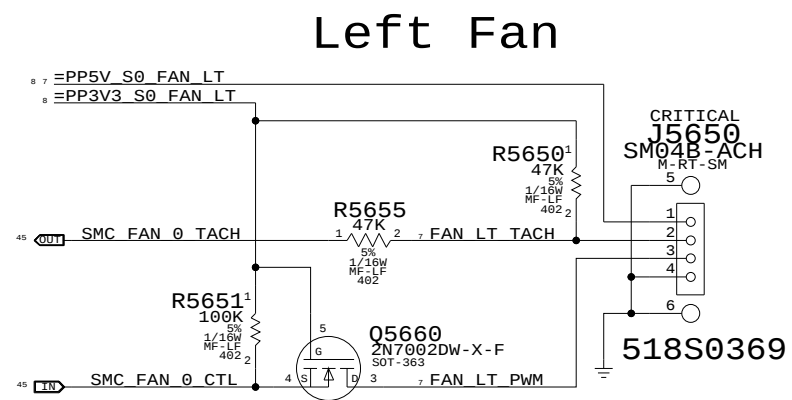
Placement note:
Keep 2 caps as close to connectors as possible

Placement note:
Keep 2 caps as close to IC pins as possible

[illegible]

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 51	OF 89





Fan Connectors

SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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APPLE INC.

SIZE
D

SIZE	DRAWING NUMBER
------	----------------

051-7413

Y.	
----	--

11.0.0

SCALE

NONE

SHT	5.0
-----	-----

52

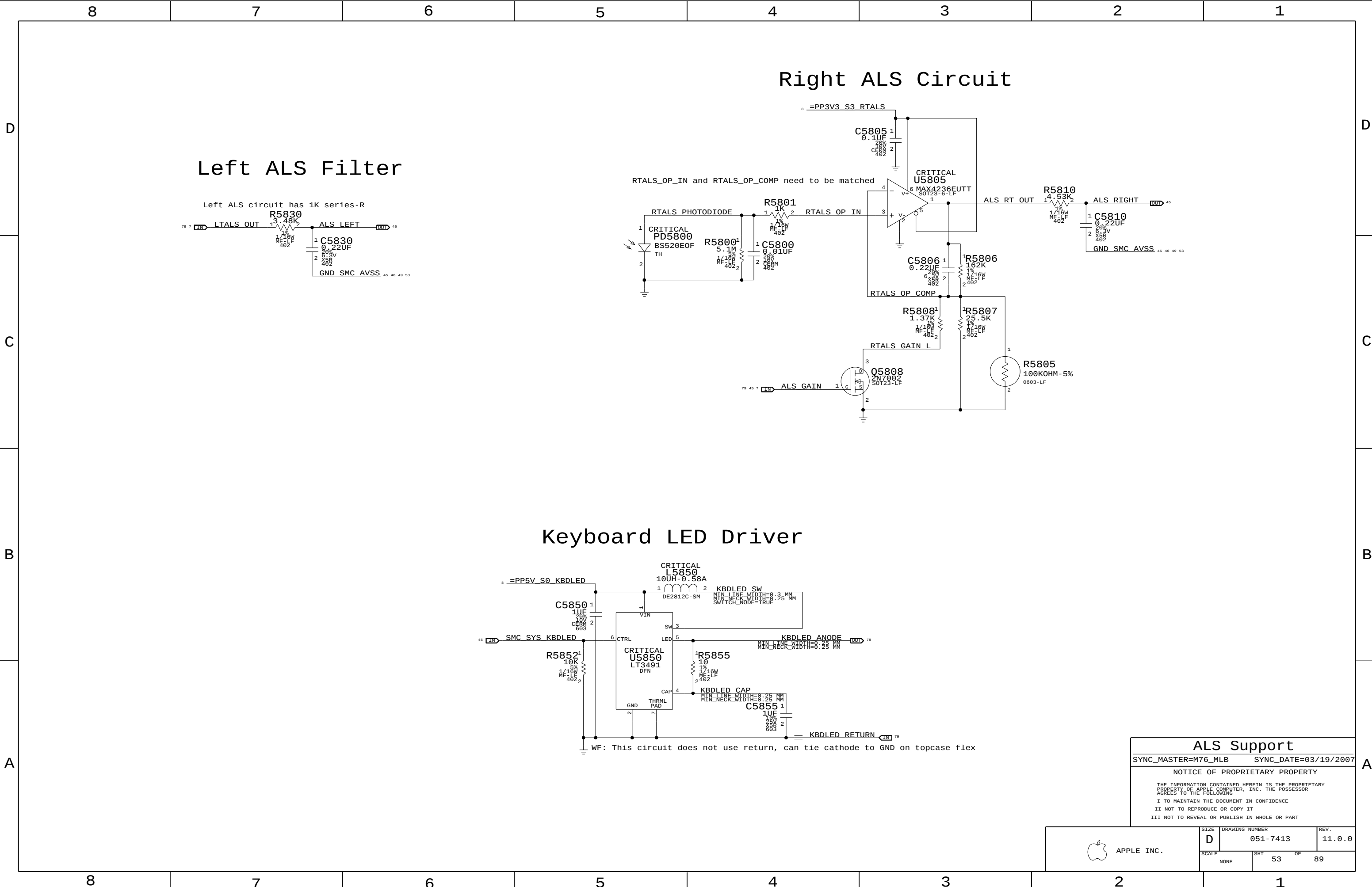
22

89

100

--	--

1



Left ALS Filter

Right ALS Circuit

Keyboard LED Driver

ALS Support

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

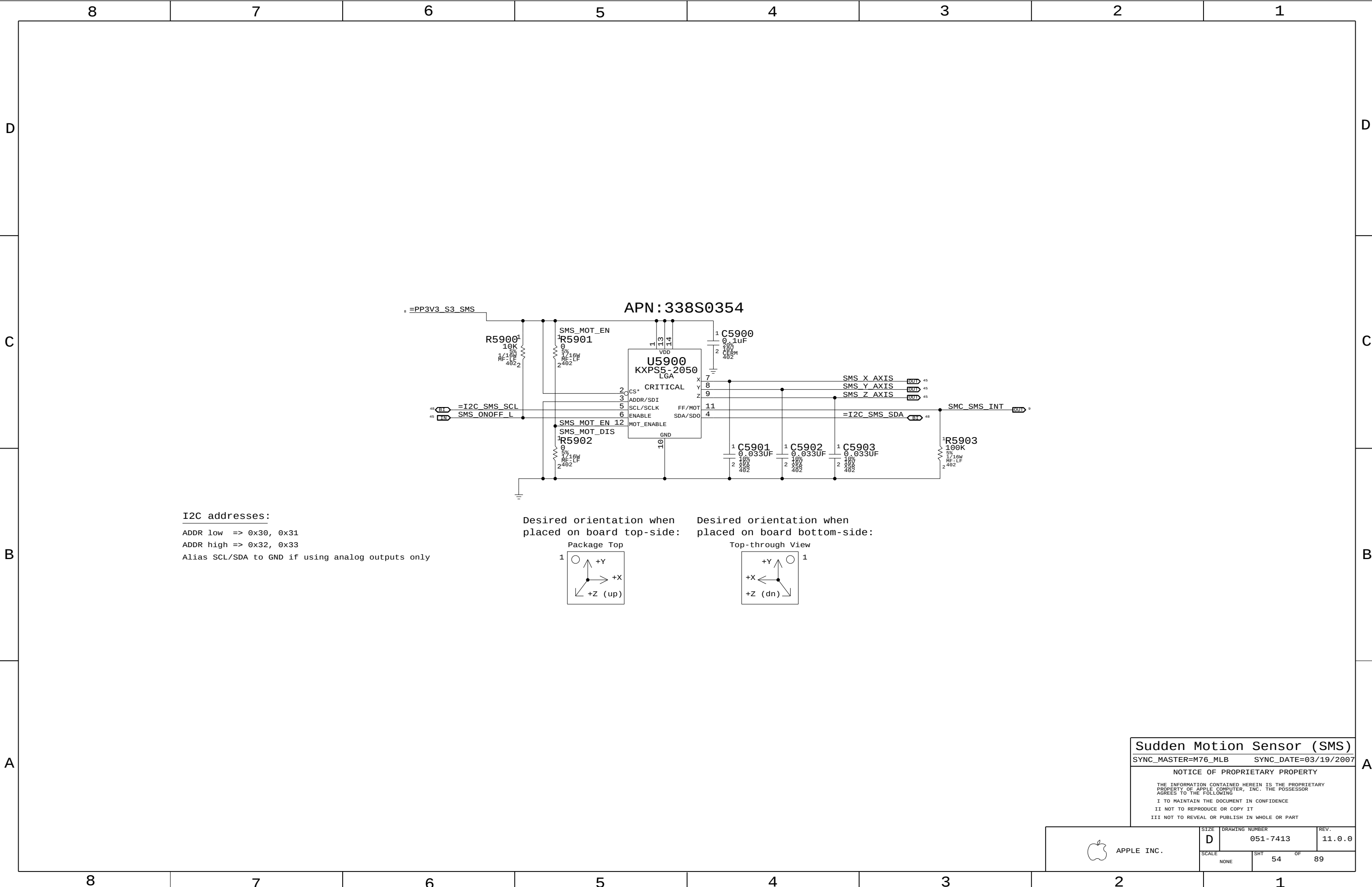
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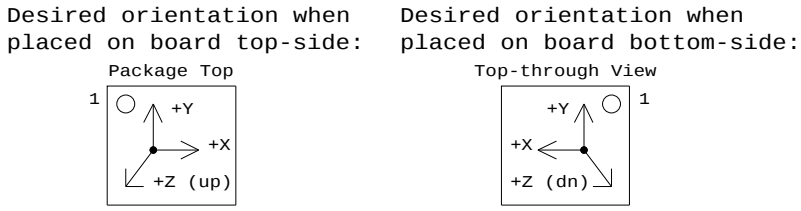
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		53	89

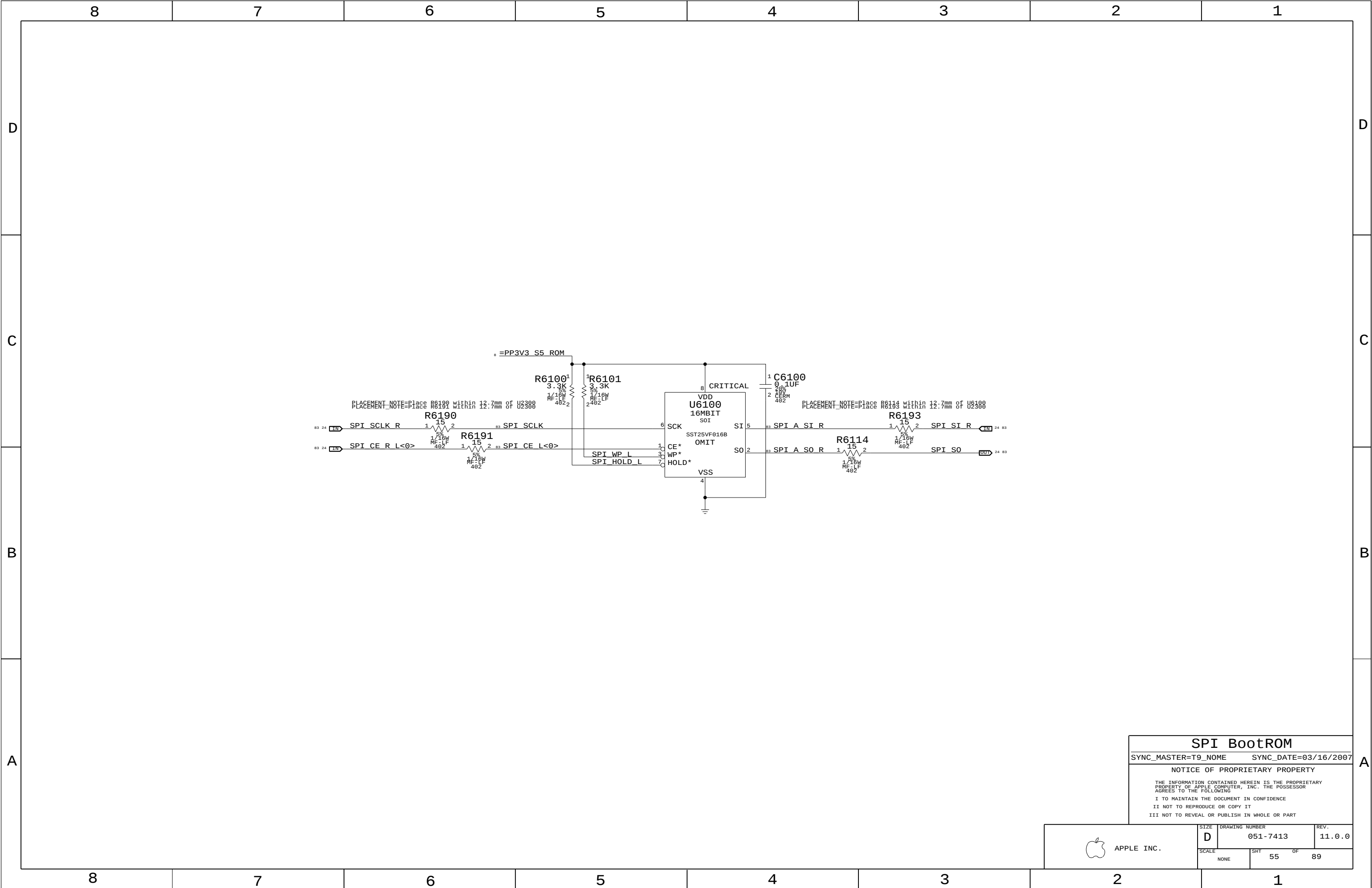


I2C addresses:
ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only



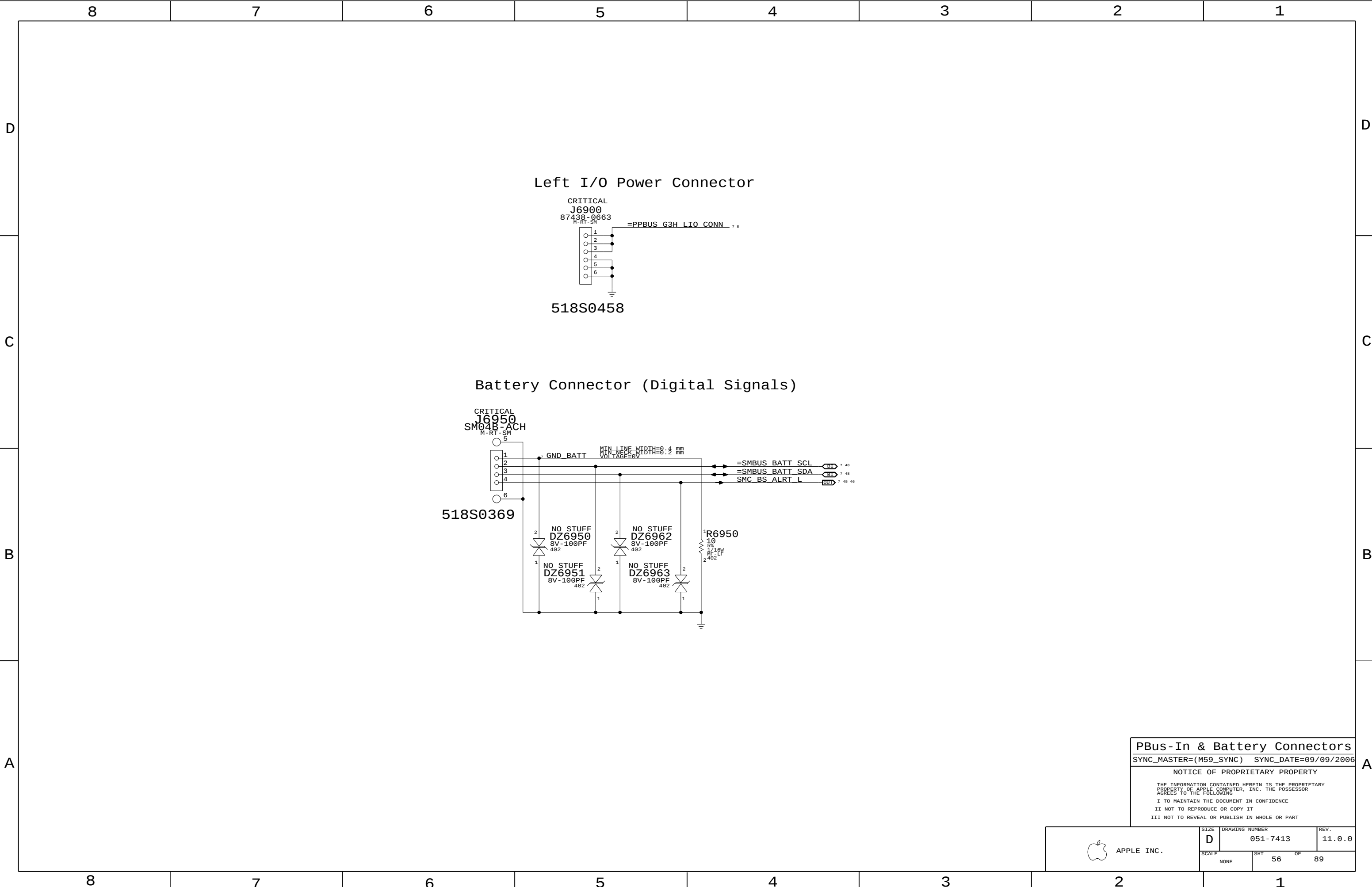
Sudden Motion Sensor (SMS)
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 54	OF 89



SPI BootROM		
SYNC_MASTER=T9_NOME		SYNC_DATE=03/16/2007
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SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
SCALE NONE	SHT 55	OF 89

 APPLE INC.
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PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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APPLE INC.

SIZE
D

DRAWING NUMBER

051-7413

REV.

11.0.0

SCALE

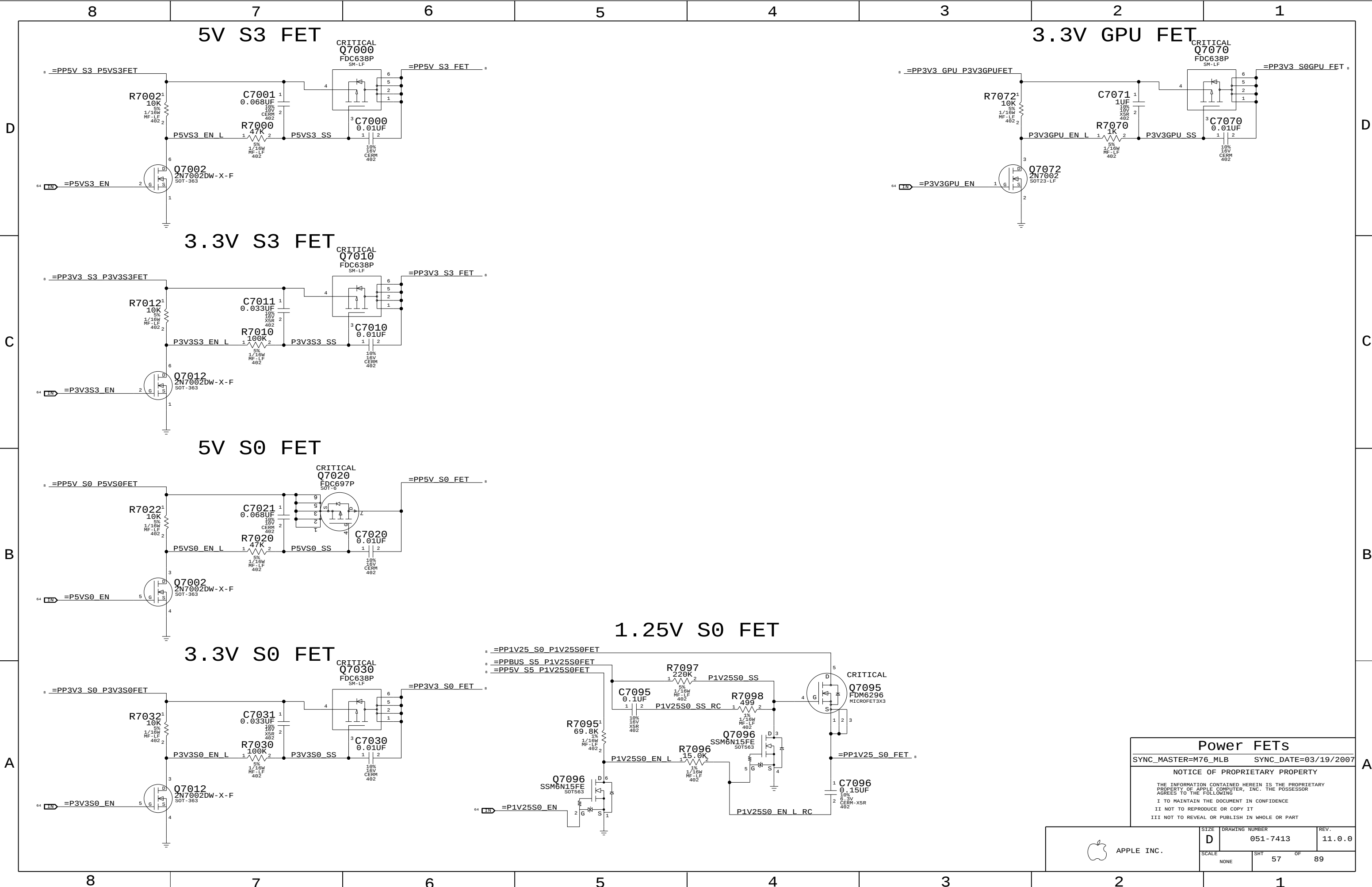
NONE

SHT

56

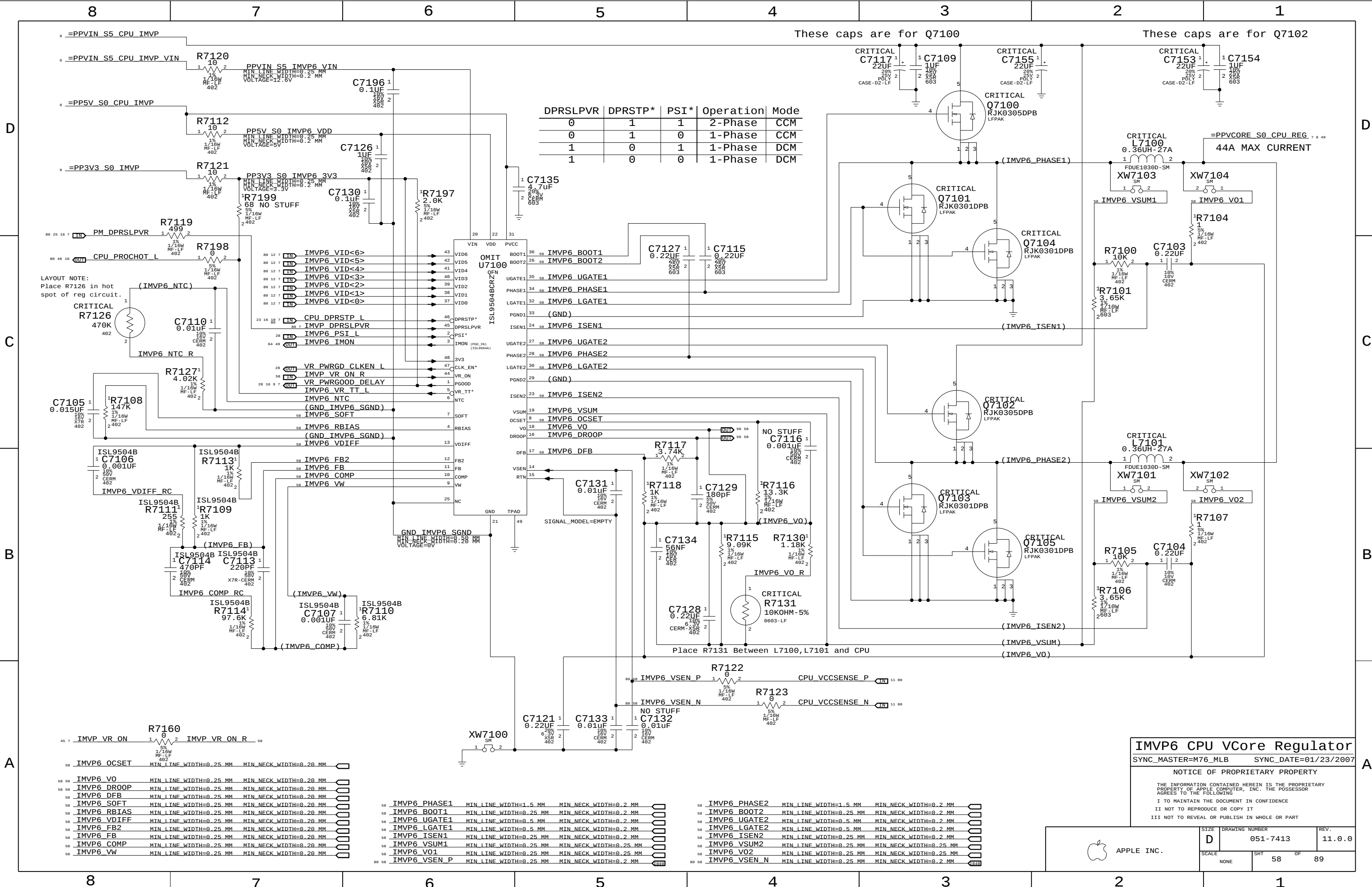
OF

89



Power FETs
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		57	89



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

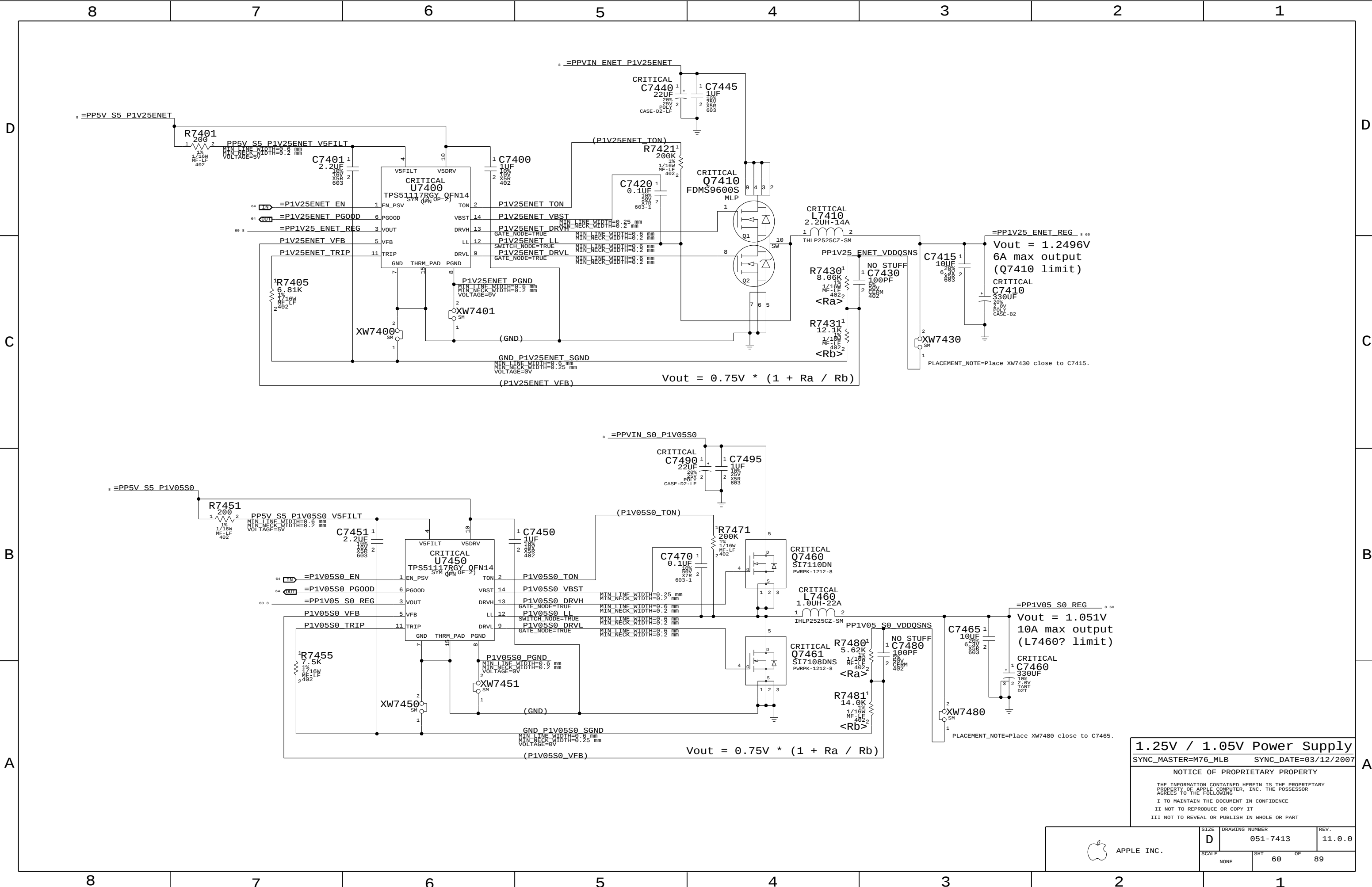
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	58	89



1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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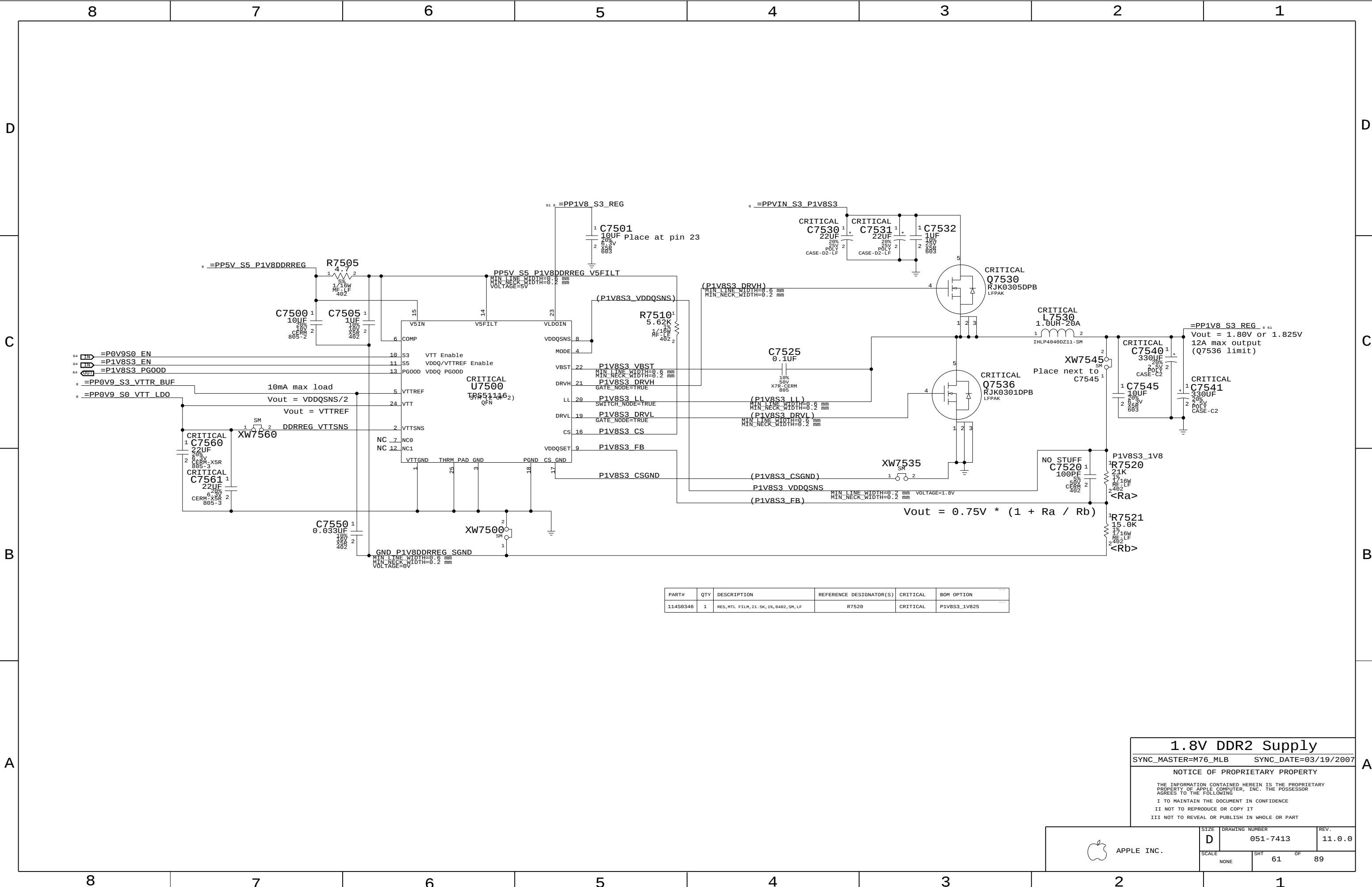
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	60	89



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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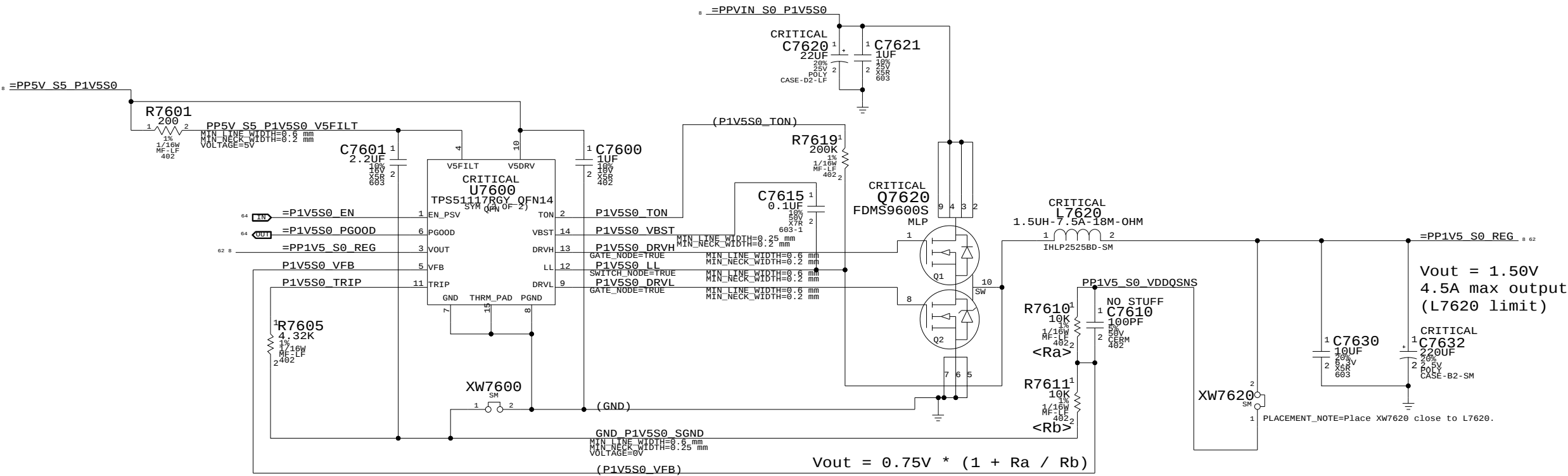
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE D DRAWING NUMBER 051-7413 REV. 11.0.0

SCALE NONE SHT 61 OF 89



1.5V Power Supply

SYNC_MASTER=M76_MLB

SYNC_DATE=03/12/2007

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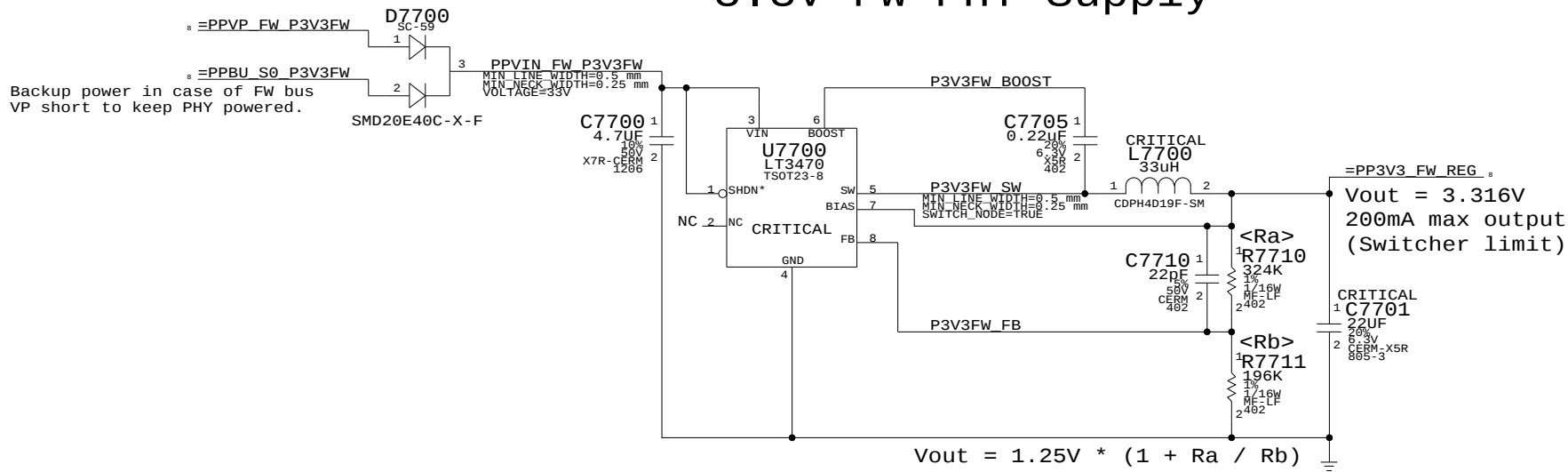
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II NOT TO REPRODUCE OR COPY IT

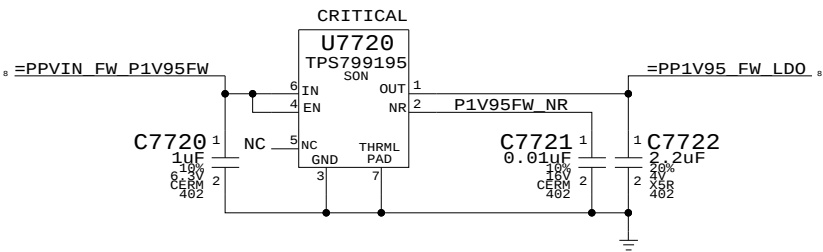
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		62	89

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7413

REV.

11.0.0

SCALE

NONE

SHT

63

OF

89

Power Control Signals

3.425V "G3Hot" Supply

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Supply needs to guarantee 3.31V delivered to SMC Vref generator

Vout = 3.425
200mA max output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

Unused PG00D Signals

- =P1V25ENET PG00D == TP P1V25ENET PG00D
- =P1V8_S0GPU PG00D == TP P1V8_S0GPU PG00D

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

NOTE: 0.9V is not checked!
Other S0 Rails PWRGD Circuit

3.425V G3Hot Supply & Power Control
SYNC_MASTER=M88 SYNC_DATE=08/02/2007

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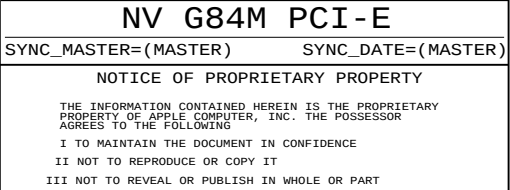
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	64	89

```
Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
```

```
Signal aliases required by this page:
(NONE)
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```
BOM options provided by this page:
(NONE)
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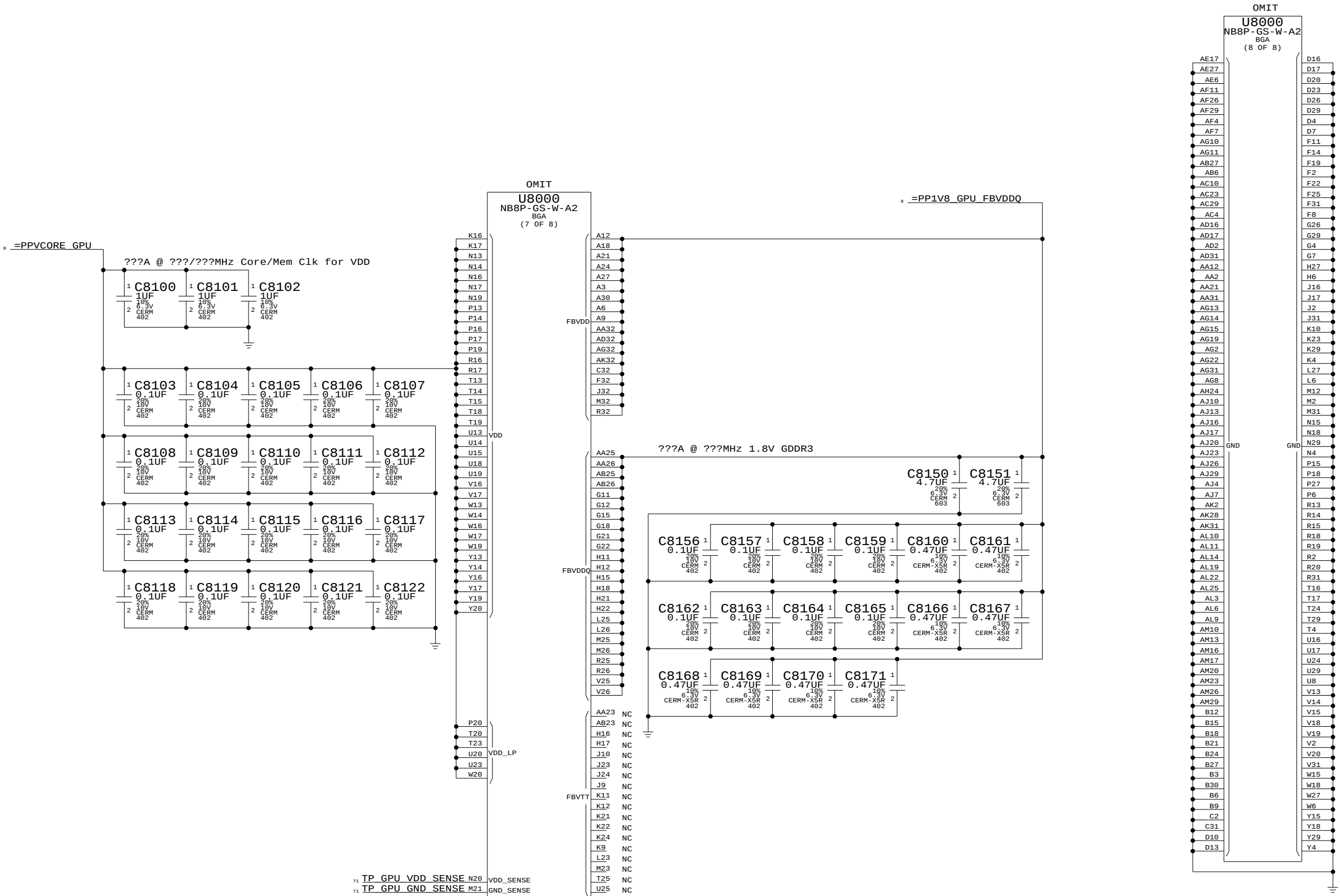
SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
SCALE NONE	SHT 65	OF 89

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	66	89

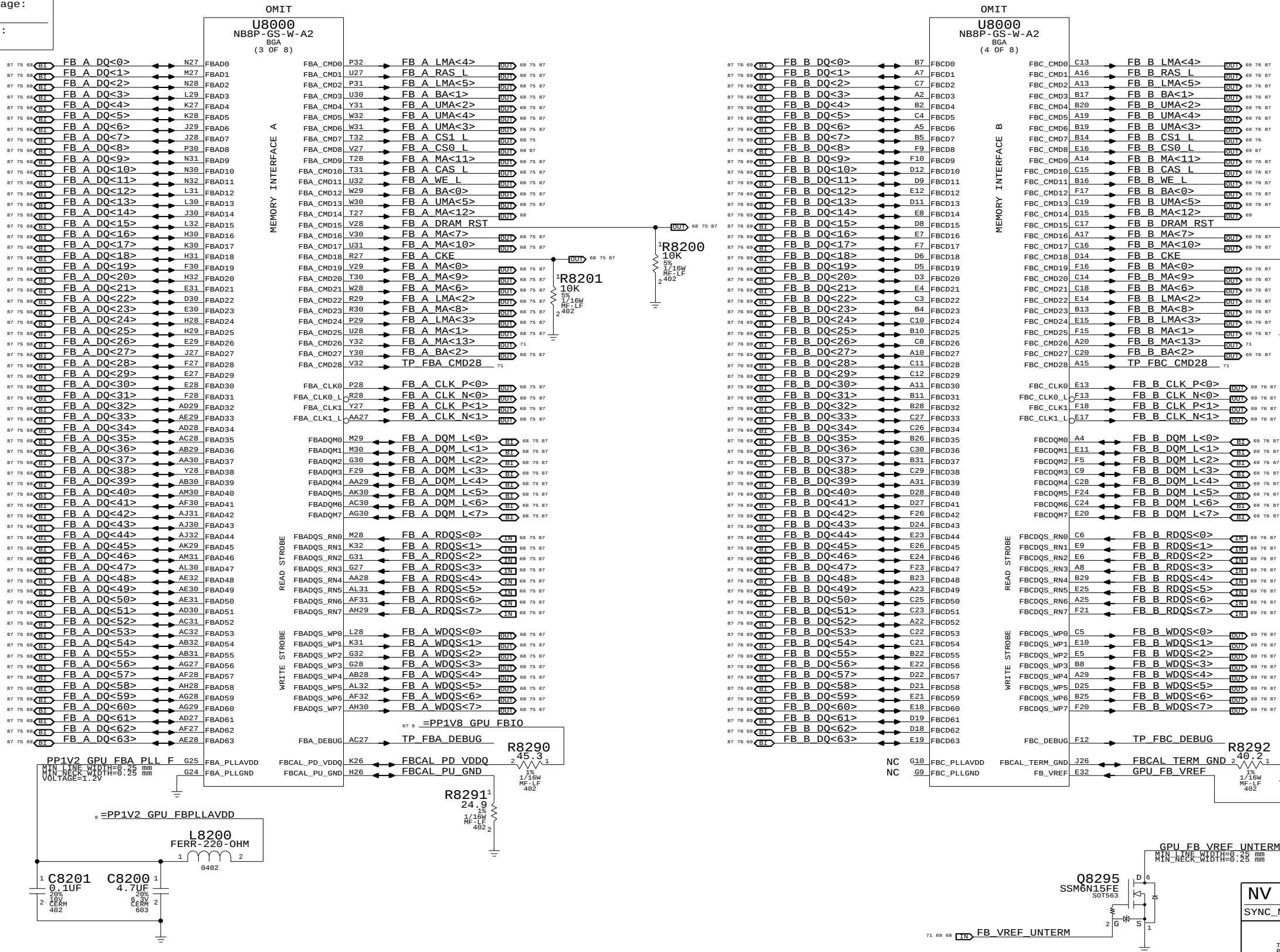
Page Notes

Power aliases required by this page:

- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBI0

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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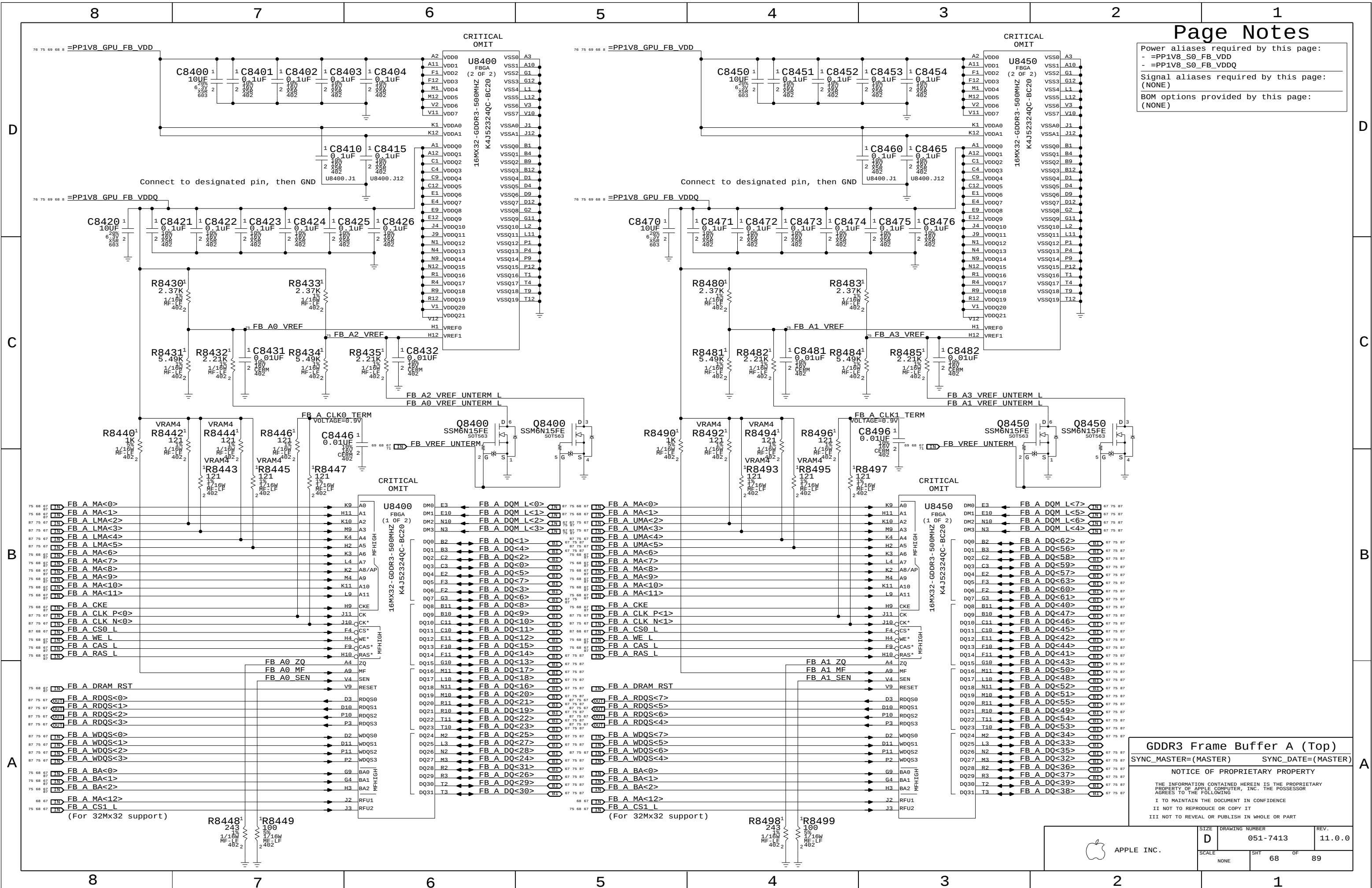
SIZE D
DRAWING NUMBER 051-7413
REV. 11.0.0
SCALE NONE
SHT 67 OF 89

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	68	89

Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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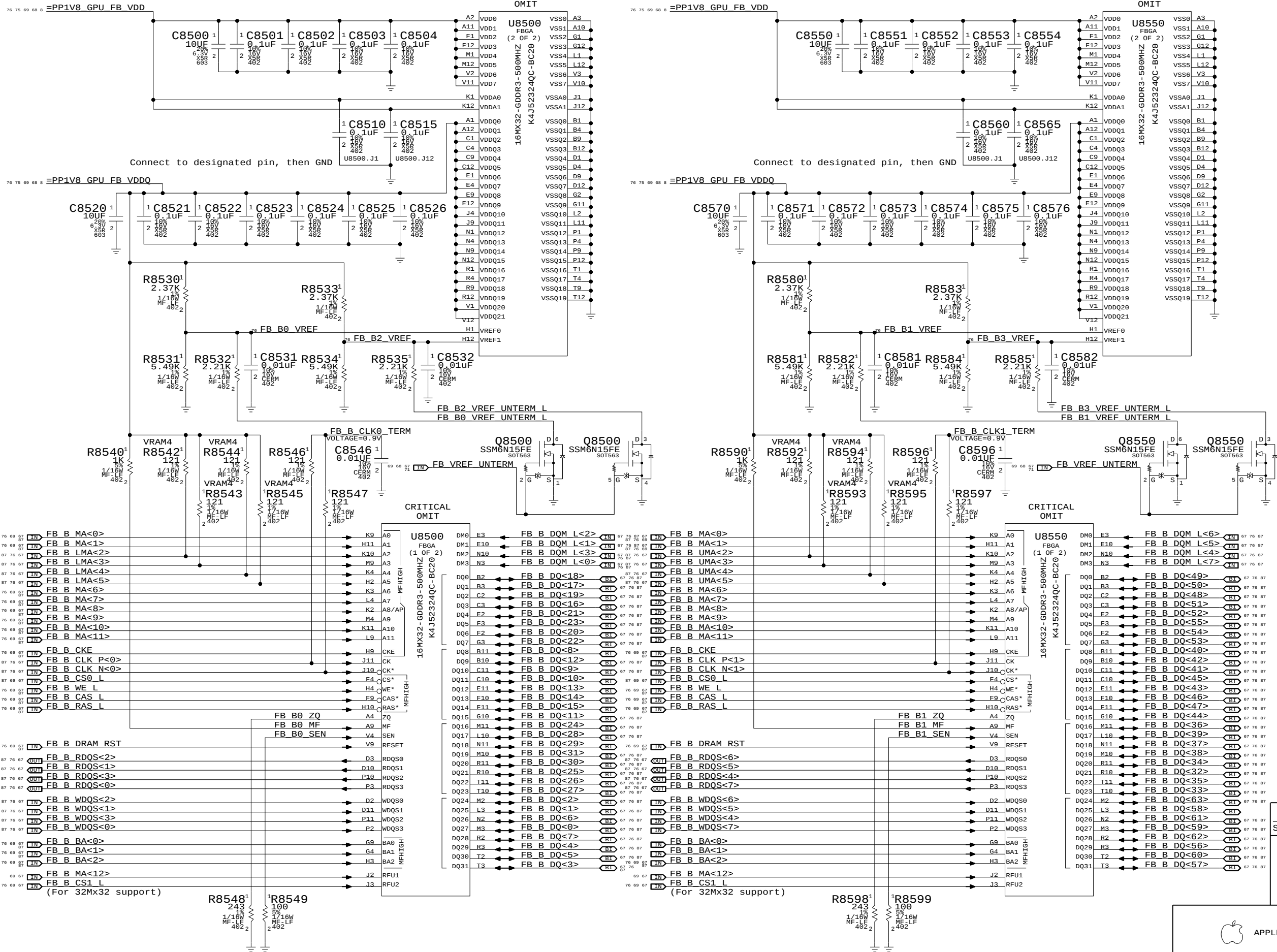
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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	69	89

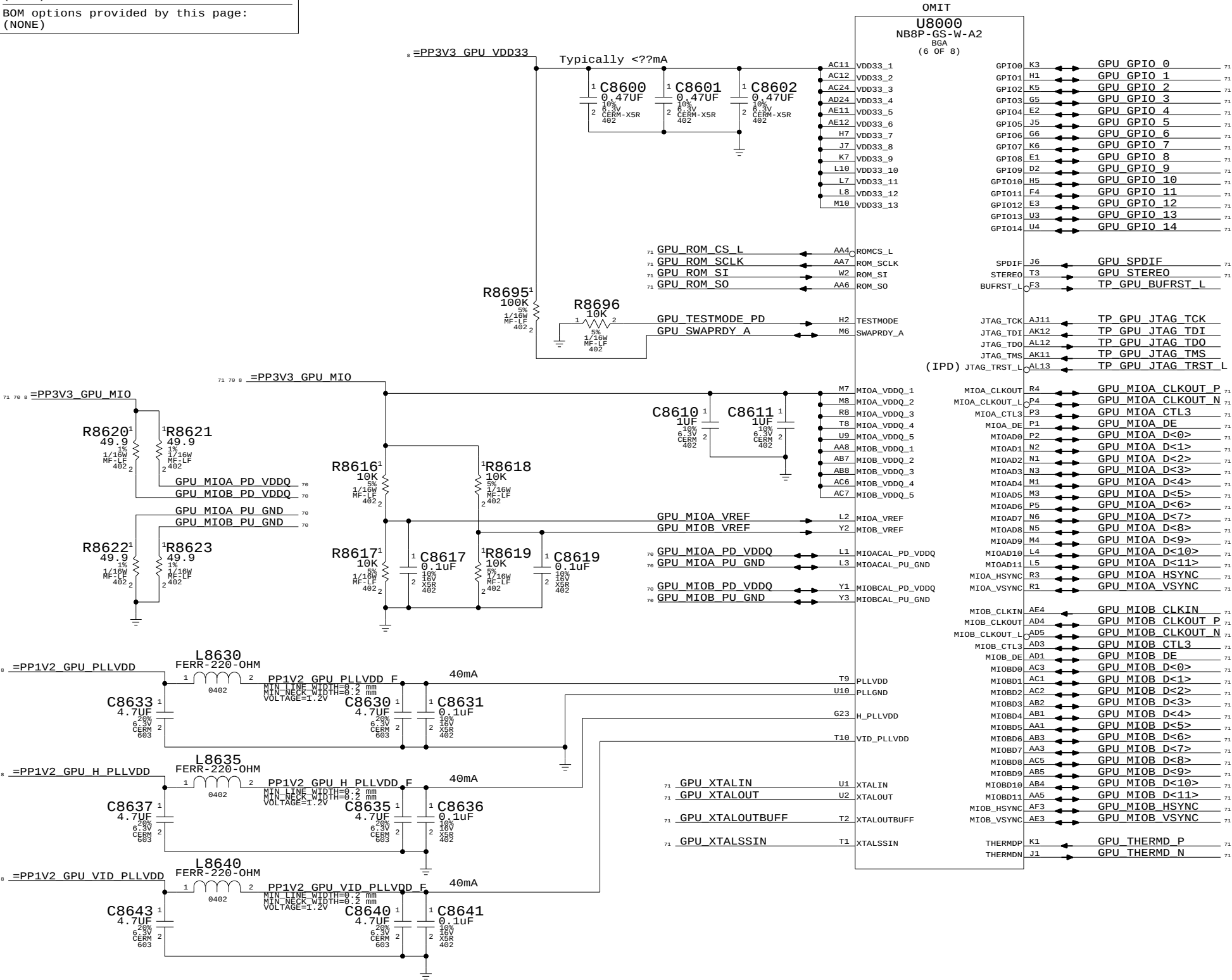


Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

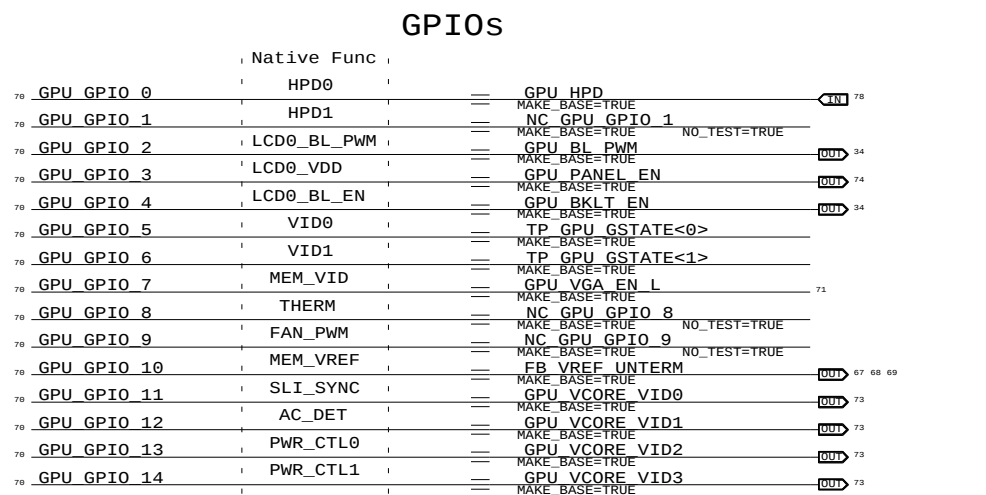
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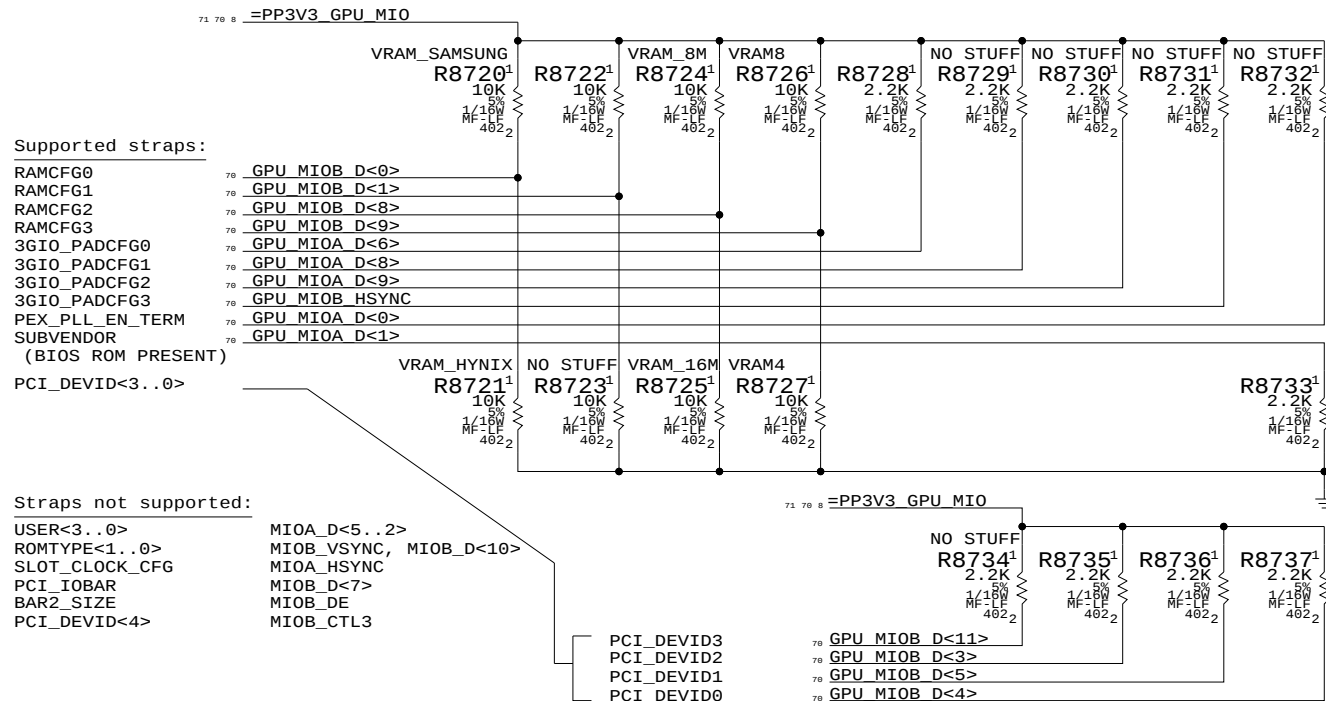


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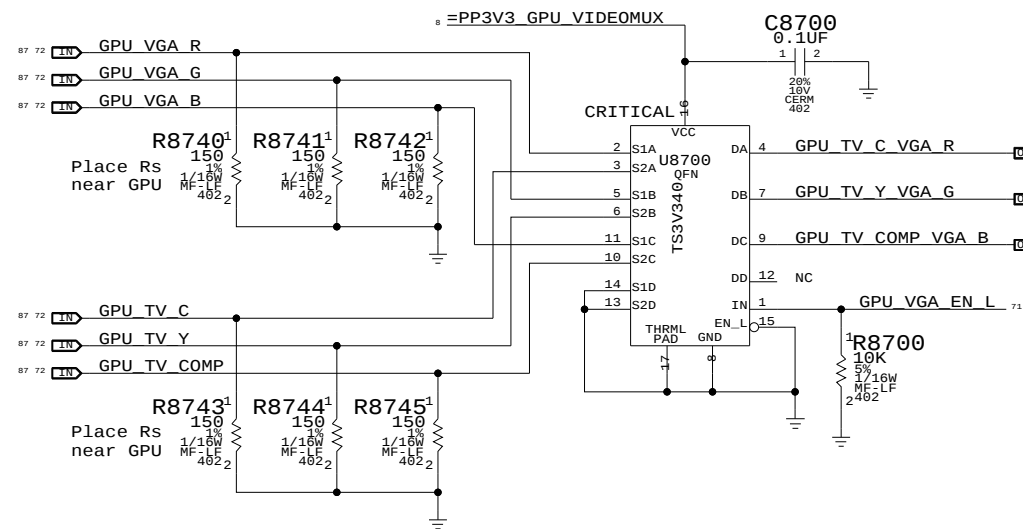
SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	70	89



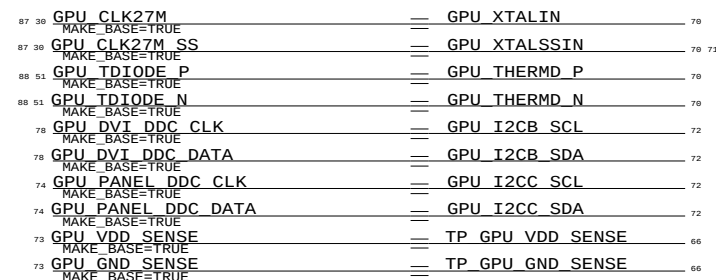
Config Straps



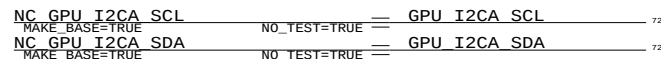
Analog Video Mux



Renamed signals

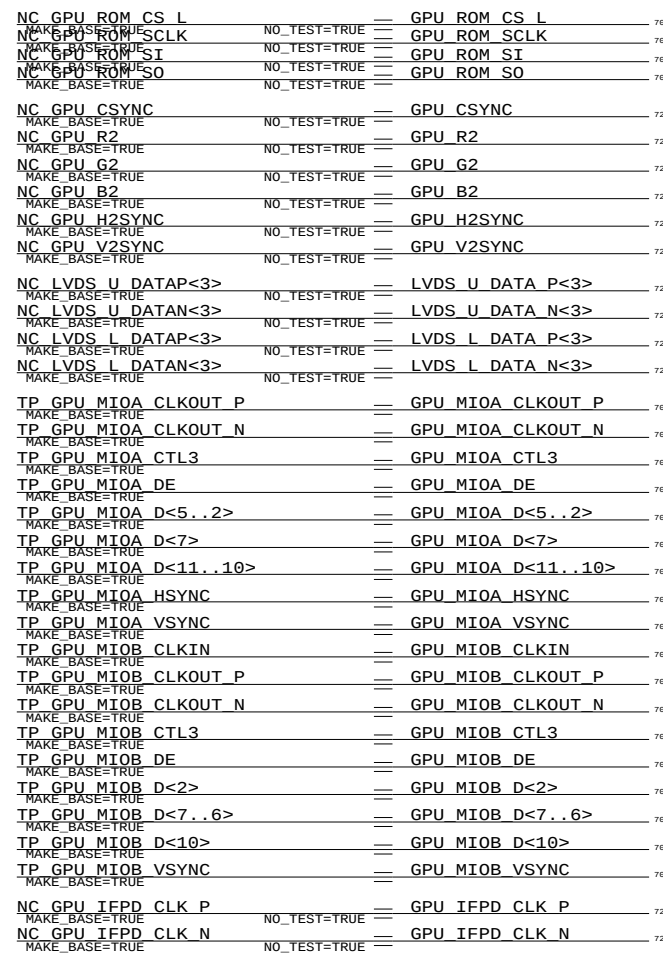
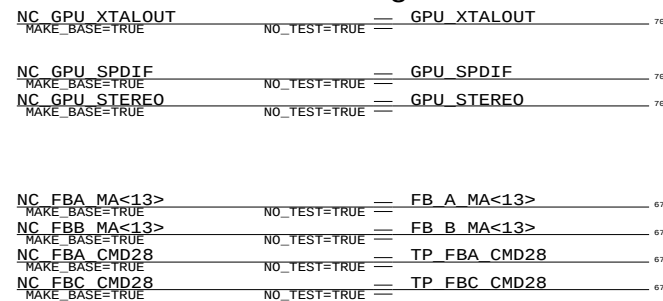


Unused I2C Buses

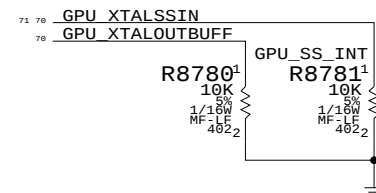


I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals



Unused Clocks



GPU Straps

SYNC_MASTER=M88	SYNC_DATE=08/02/2007
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SIZE

DRAWING NUMBER

REV.	11.0.0
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SCALE

NONE

	SHT
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HT

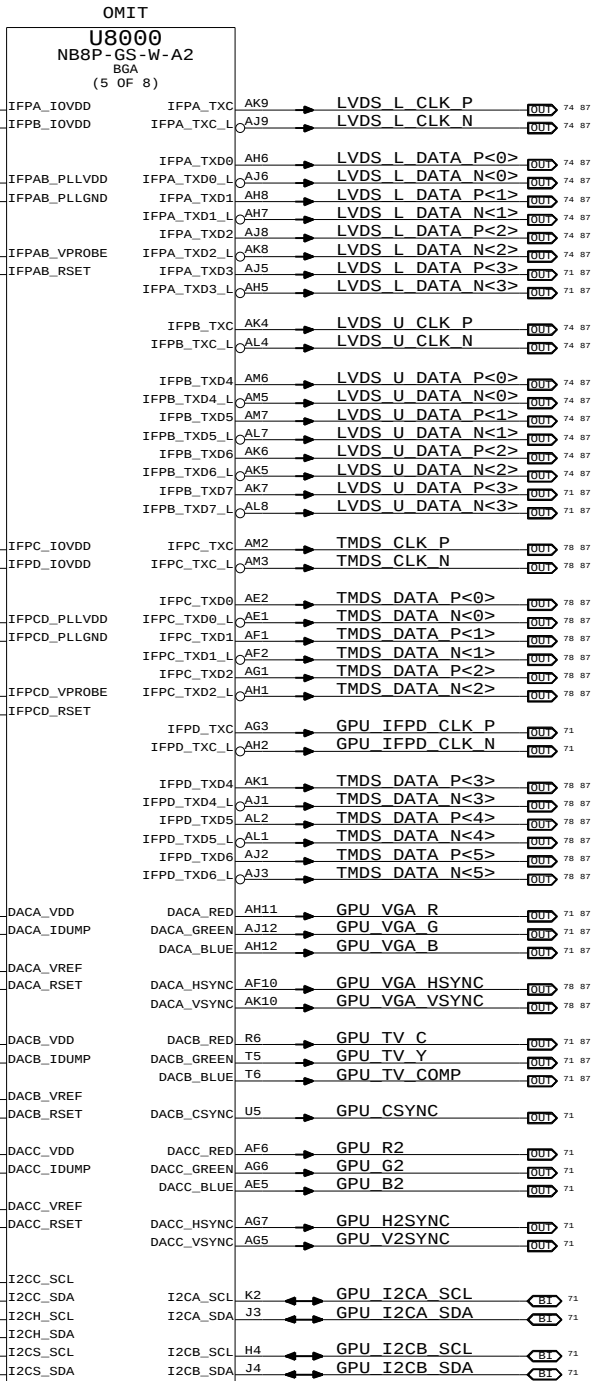
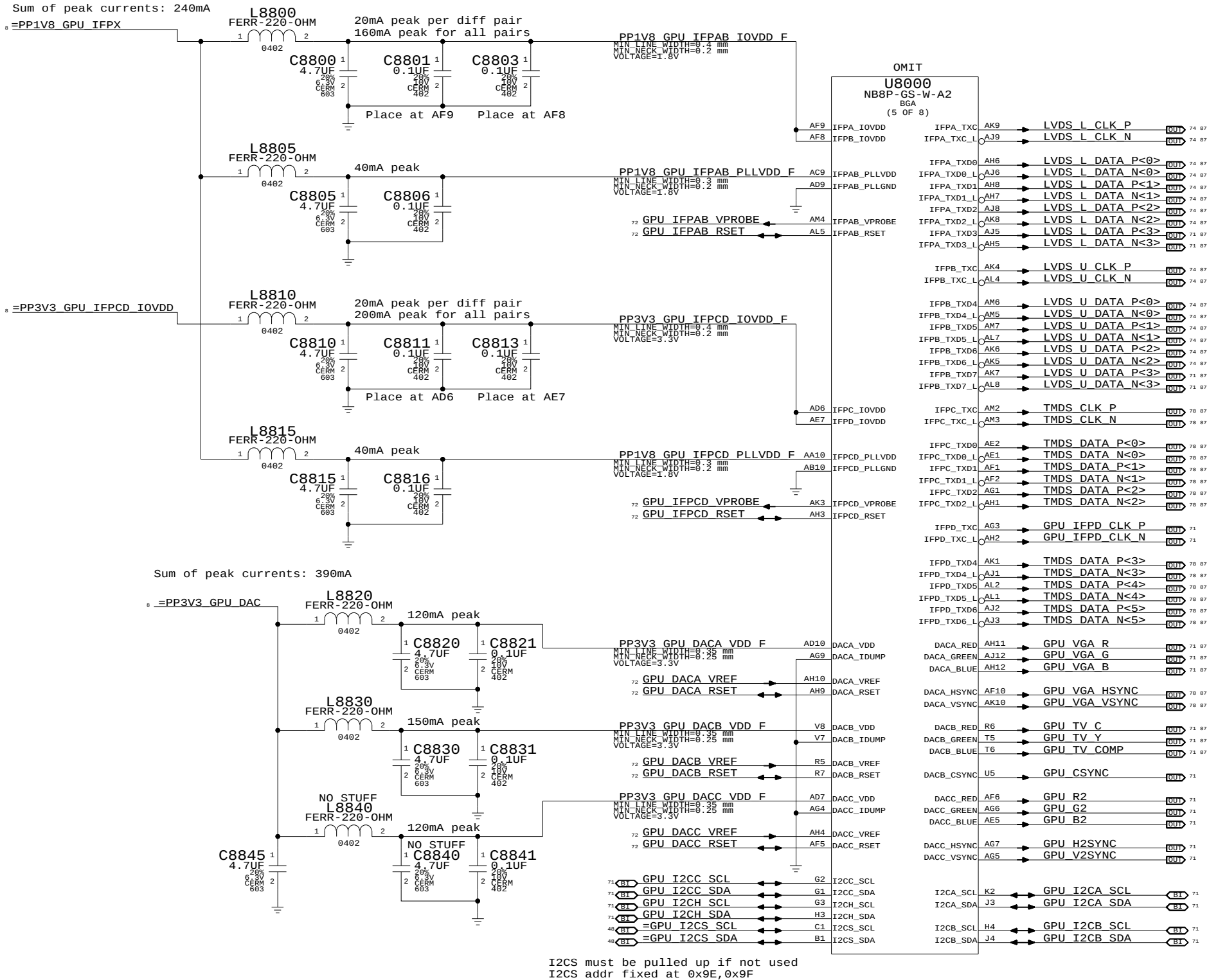
89

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

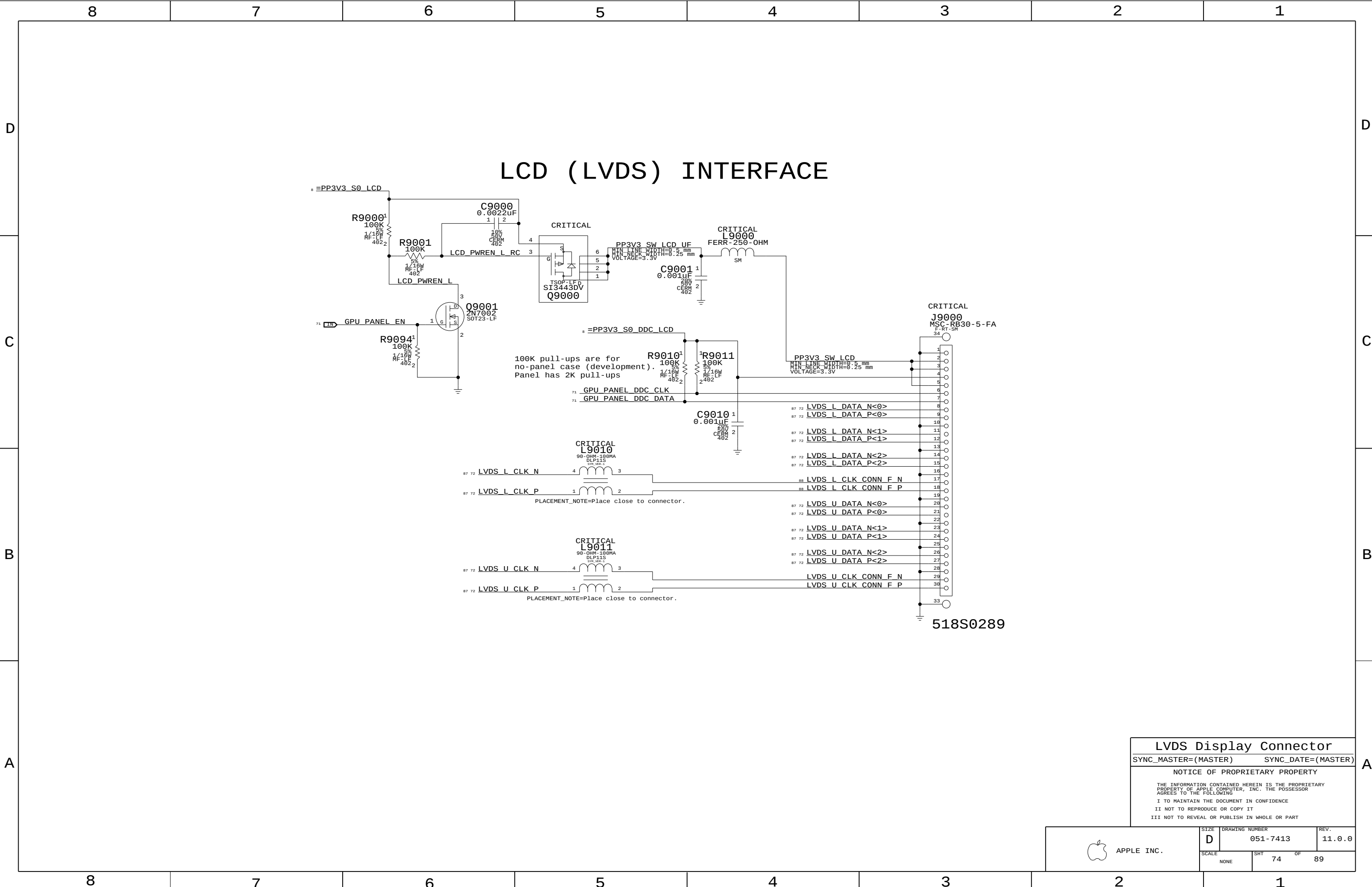
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	72	89



LVDS Display Connector
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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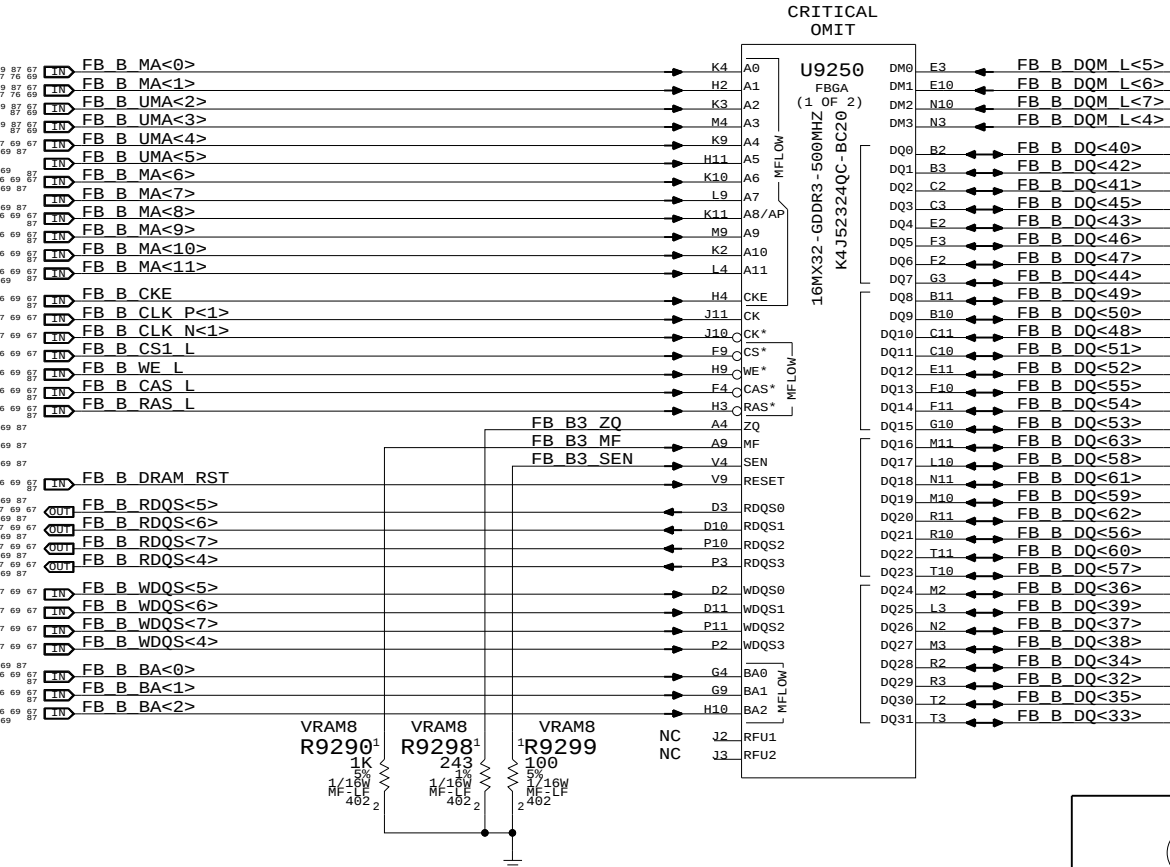
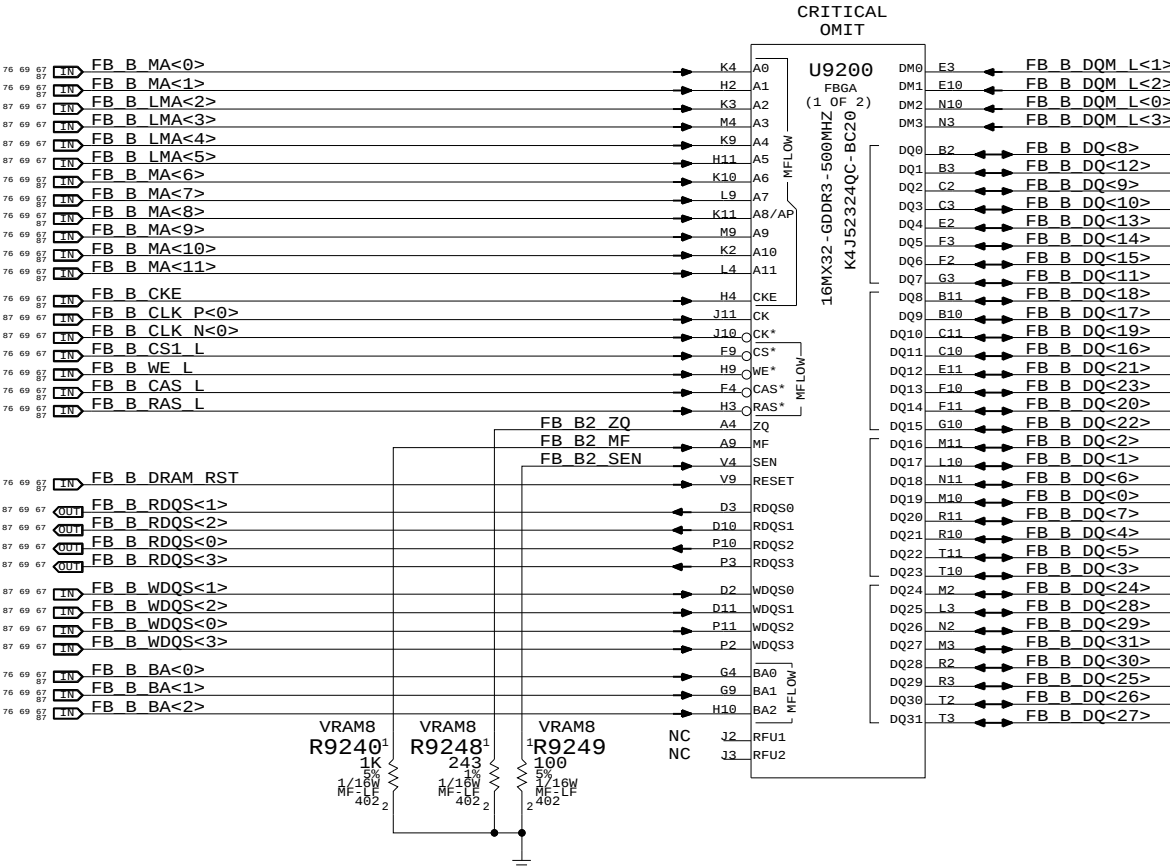
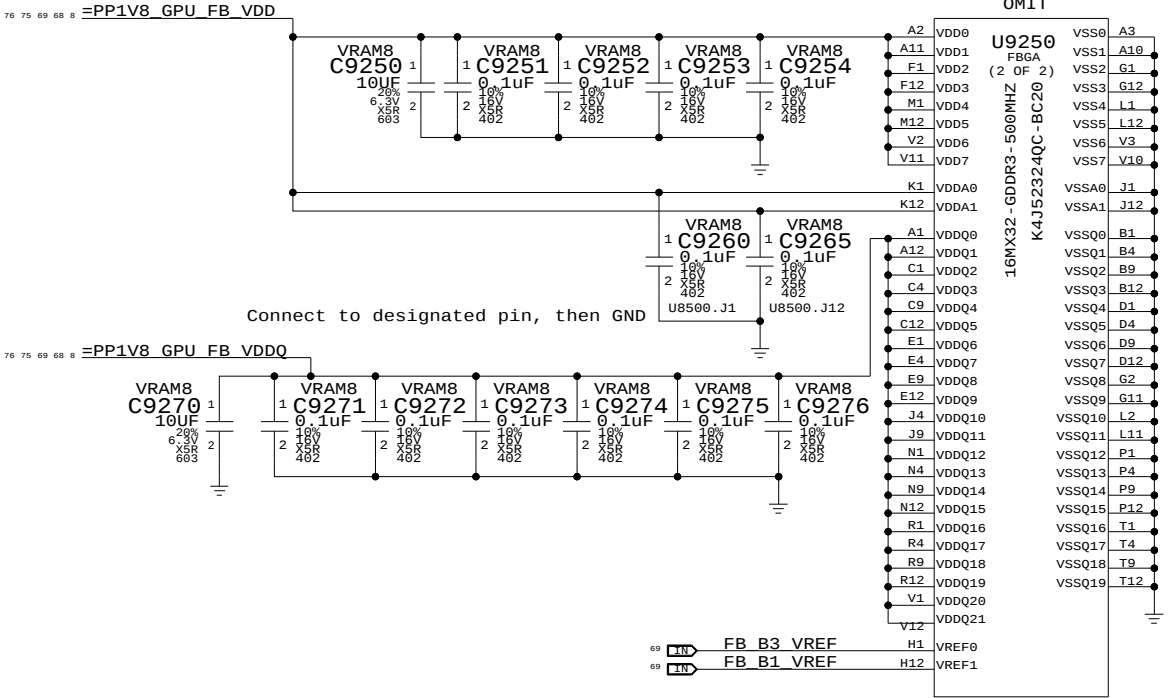
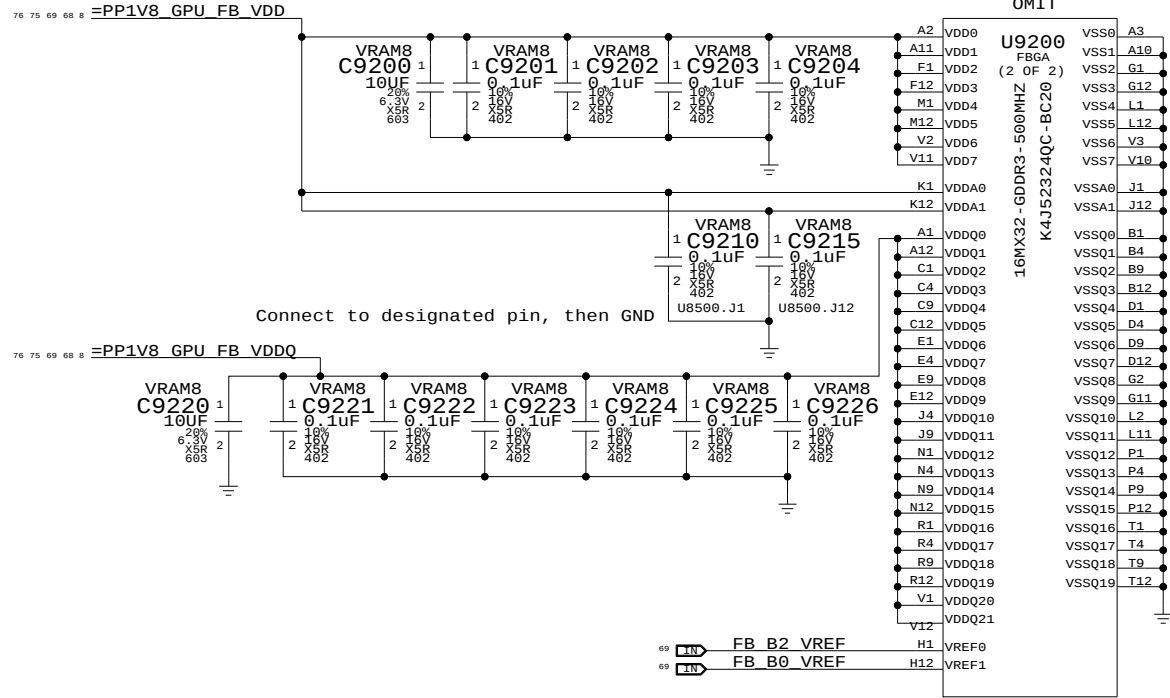
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		74	89

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M88_MLB_VRAMS0C_DATE=06/19/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7413

REV.

11.0.0

SCALE

NONE

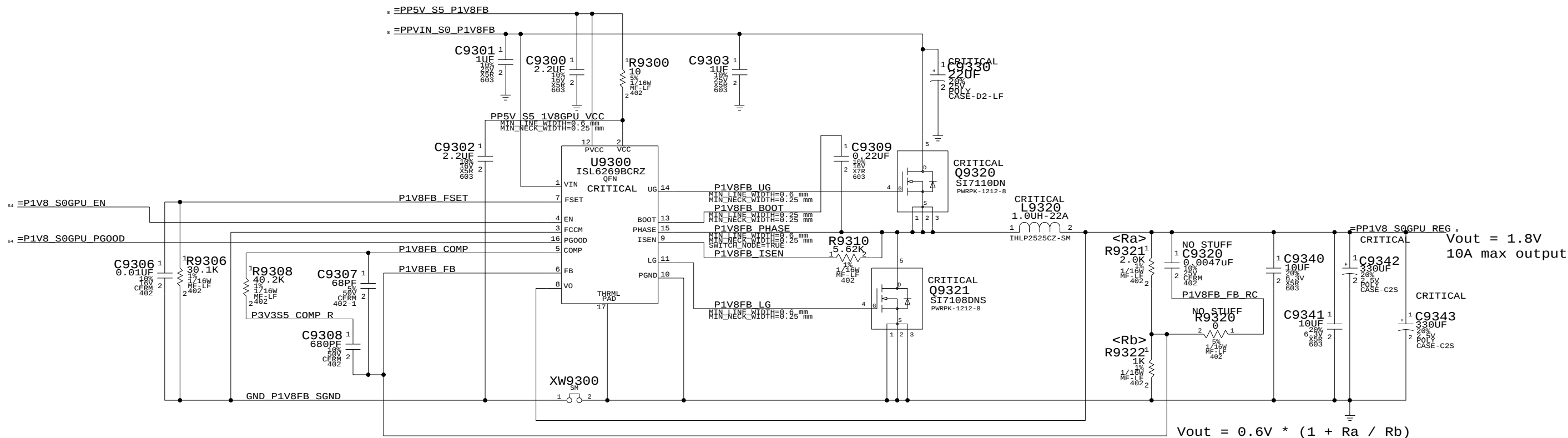
SHT

76

OF

89

1.8V Frame Buffer Regulator



1.8V FB Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

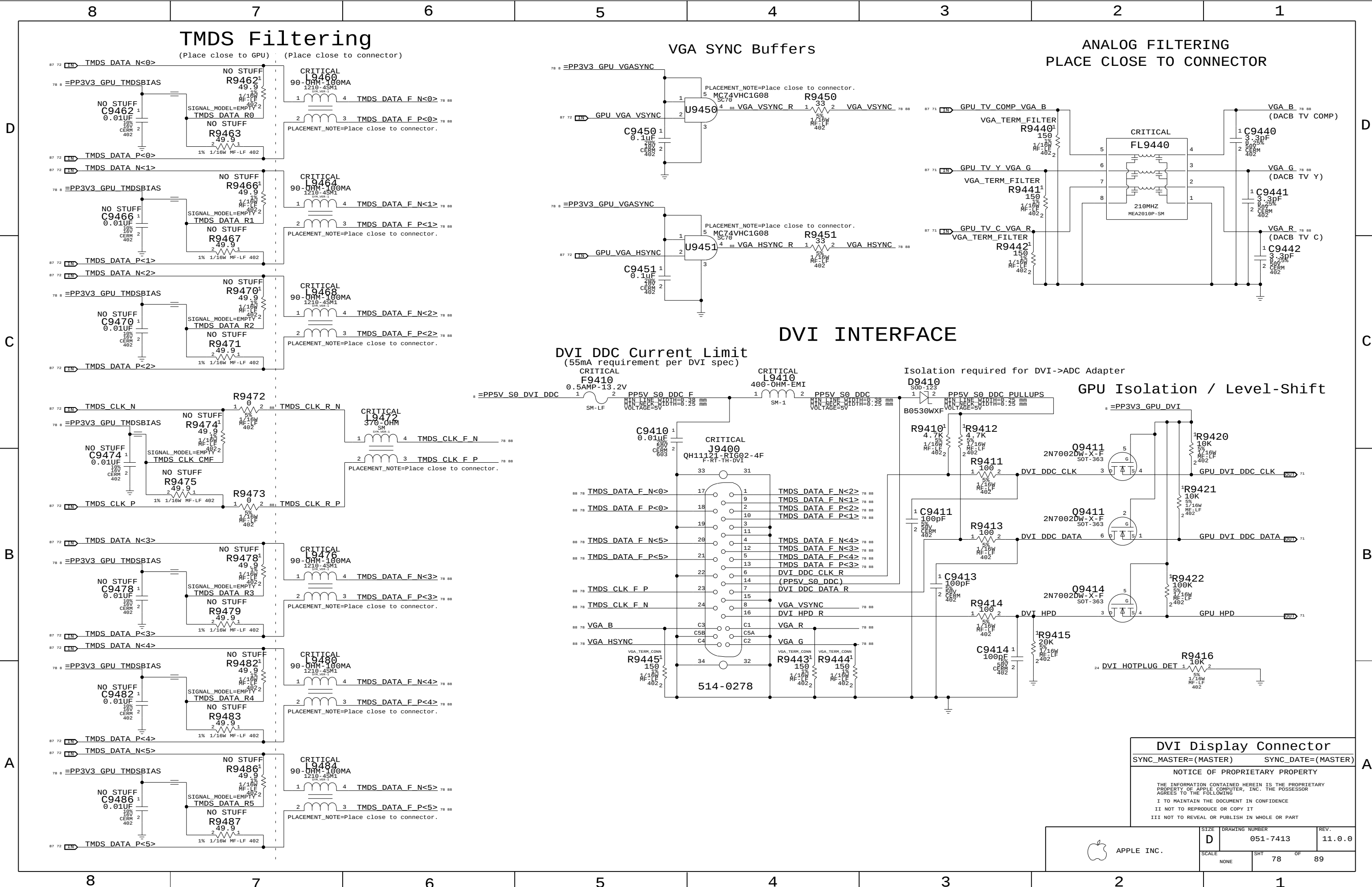
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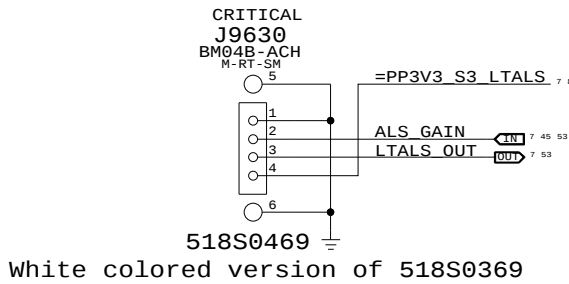
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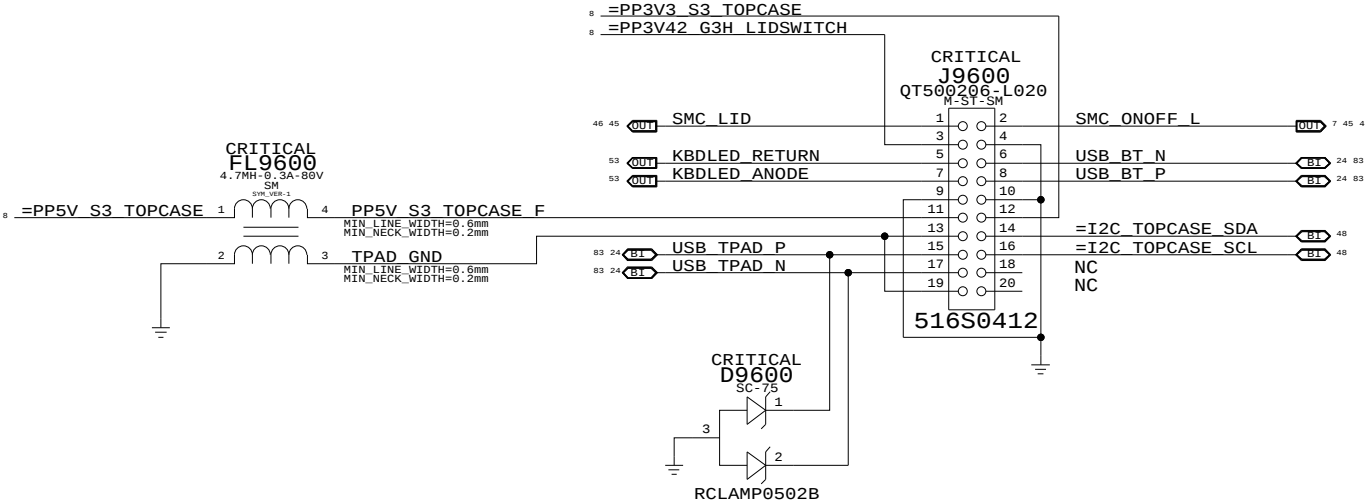
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		77	89



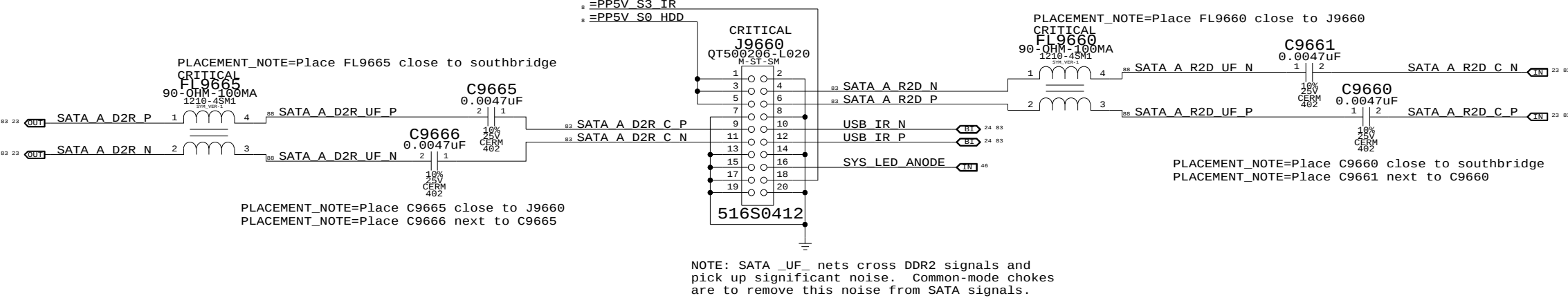
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



Project Specific Connectors
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 79	OF 89

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB _{min} COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRT L	10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
	FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
	FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DTNV L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DTNV L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DTNV L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DTNV L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
	FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
	FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
	CPU_IERR_L	CPU_55S		CPU IERR L	10
	CPU_FERR_L	CPU_55S		CPU FERR L	10 23
	CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 58
	CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
	CPU_FROM_SB	CPU_55S		CPU INTR	10 23
	CPU_FROM_SB	CPU_55S		CPU NMI	10 23
	CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
	CPU_FROM_SB	CPU_55S		CPU DPSLP L	7 10 23
	CPU_FROM_SB	CPU_55S		CPU IGNE L	10 23
	CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
	CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
	CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 23
	PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
	FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
	PM DPRSLPVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 58
	(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 58
	CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
	(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
	CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
	(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
	CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
	(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
	CPU DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 58
	CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
	CPU_COMP	CPU_55S		CPU COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
	CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
	XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
	XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
	XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
	XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
	XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
	XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
	XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
	CLK_FSB_100D	CLK_FSB		XDP CLK P	13 30 85
	CLK_FSB_100D	CLK_FSB		XDP CLK N	13 30 85
	(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
		CPU_55S	CPU_2T01	CPU VID<6..0>	11 12
		CPU_55S	CPU_2T01	IMVP6_VID<6..0>	7 12 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 58
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN P	58
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007
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D	051-7413	11.0.0

SCALE	SHT	OF
NONE	80	89

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNT1	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNT1	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNT1	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNT1	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNT1	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNT1	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNT1	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	24
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	24
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	9 24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME SYNC_DATE=01/17/2007

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_46SE	*	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>
		GDDR3_80D	GDDR3_CLK	FB A CLK N<0>
	FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>
		GDDR3_80D	GDDR3_CLK	FB A CLK N<1>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<11..6>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A RAS_L
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CAS_L
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A WE_L
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A CKE
	FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB A CS0_L
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM_RST
	FB_A_CMD	GDDR3_46SE	GDDR3_CMD	FB A LMA<5..2>
	FB_B_CMD	GDDR3_46SE	GDDR3_CMD	FB A UMA<5..2>
	FB_A_WDQS0	GDDR3_46SF	GDDR3_DQS	FB A WDQS<0>
	FB_A_WDQS1	GDDR3_46SE	GDDR3_DQS	FB A WDQS<1>
	FB_A_WDQS2	GDDR3_46SE	GDDR3_DQS	FB A WDQS<2>
	FB_A_WDQS3	GDDR3_46SE	GDDR3_DQS	FB A WDQS<3>
	FB_A_RDQS0	GDDR3_46SE	GDDR3_DQS	FB A RDQS<0>
	FB_A_RDQS1	GDDR3_46SE	GDDR3_DQS	FB A RDQS<1>
	FB_A_RDQS2	GDDR3_46SE	GDDR3_DQS	FB A RDQS<2>
	FB_A_RDQS3	GDDR3_46SE	GDDR3_DQS	FB A RDQS<3>
	FB_A_DQ_BYTE0	GDDR3_46SF	GDDR3_DATA	FB A DQ<7..0>
	FB_A_DQ_BYTE1	GDDR3_46SF	GDDR3_DATA	FB A DQ<15..8>
	FB_A_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB A DQ<23..16>
	FB_A_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB A DQ<31..24>
	FB_A_DQM0	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<0>
	FB_A_DQM1	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<1>
	FB_A_DQM2	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<2>
	FB_A_DQM3	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<3>
	FB_B_WDQS0	GDDR3_46SE	GDDR3_DQS	FB A WDQS<4>
	FB_B_WDQS1	GDDR3_46SE	GDDR3_DQS	FB A WDQS<5>
	FB_B_WDQS2	GDDR3_46SE	GDDR3_DQS	FB A WDQS<6>
	FB_B_WDQS3	GDDR3_46SE	GDDR3_DQS	FB A WDQS<7>
	FB_B_RDQS0	GDDR3_46SE	GDDR3_DQS	FB A RDQS<4>
	FB_B_RDQS1	GDDR3_46SE	GDDR3_DQS	FB A RDQS<5>
	FB_B_RDQS2	GDDR3_46SE	GDDR3_DQS	FB A RDQS<6>
	FB_B_RDQS3	GDDR3_46SE	GDDR3_DQS	FB A RDQS<7>
	FB_B_DQ_BYTE0	GDDR3_46SF	GDDR3_DATA	FB A DQ<39..32>
	FB_B_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB A DQ<47..40>
	FB_B_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB A DQ<55..48>
	FB_B_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB A DQ<63..56>
	FB_B_DQM0	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<4>
	FB_B_DQM1	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<5>
	FB_B_DQM2	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<6>
	FB_B_DQM3	GDDR3_46SE	GDDR3_DATA	FB A DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>	67 69 76
		GDDR3_80D	GDDR3_CLK	FB B CLK N<0>	67 69 76
	FB_D_CLK_P	GDDR3_80D	GDDR3_CLK_P	FB B CLK P<1>	67 69 76
		GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<1..0>	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<11..6>	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B BA<2..0>	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B CAS L	67 69 76
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L	67 69 76
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B CE	67 69 76
	FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB B CS0 L	67 69
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B DRAM_RST	67 69 76
	FB_C_CMD	GDDR3_46SE	GDDR3_CMD	FB B LMA<5..2>	67 69 76
	FB_D_CMD	GDDR3_46SE	GDDR3_CMD	FB B UMA<5..2>	67 69 76
	FB_C_WDQS0	GDDR3_46SF	GDDR3_DQS	FB B WDQS<0>	67 69 76
	FB_C_WDQS1	GDDR3_46SF	GDDR3_DQS	FB B WDQS<1>	67 69 76
	FB_C_WDQS2	GDDR3_46SF	GDDR3_DQS	FB B WDQS<2>	67 69 76
	FB_C_WDQS3	GDDR3_46SF	GDDR3_DQS	FB B WDQS<3>	67 69 76
	FB_C_RDQS0	GDDR3_46SE	GDDR3_DQS	FB B RDQS<0>	67 69 76
	FB_C_RDQS1	GDDR3_46SE	GDDR3_DQS	FB B RDQS<1>	67 69 76
	FB_C_RDQS2	GDDR3_46SE	GDDR3_DQS	FB B RDQS<2>	67 69 76
	FB_C_RDQS3	GDDR3_46SE	GDDR3_DQS	FB B RDQS<3>	67 69 76
	FB_C_DQ_BYTE0	GDDR3_50SF	GDDR3_DATA	FB B DQ<7..0>	67 69 76
	FB_C_DQ_BYTE1	GDDR3_46SF	GDDR3_DATA	FB B DQ<15..8>	67 69 76
	FB_C_DQ_BYTE2	GDDR3_46SF	GDDR3_DATA	FB B DQ<23..16>	67 69 76
	FB_C_DQ_BYTE3	GDDR3_46SF	GDDR3_DATA	FB B DQ<31..24>	67 69 76
	FB_C_DQM0	GDDR3_46SE	GDDR3_DATA	FB B DQM L<0>	67 69 76
	FB_C_DQM1	GDDR3_46SE	GDDR3_DATA	FB B DQM L<1>	67 69 76
	FB_C_DQM2	GDDR3_46SE	GDDR3_DATA	FB B DQM L<2>	67 69 76
	FB_C_DQM3	GDDR3_46SE	GDDR3_DATA	FB B DQM L<3>	67 69 76
	FB_D_WDQS0	GDDR3_46SF	GDDR3_DQS	FB B WDQS<4>	67 69 76
	FB_D_WDQS1	GDDR3_46SF	GDDR3_DQS	FB B WDQS<5>	67 69 76
	FB_D_WDQS2	GDDR3_46SF	GDDR3_DQS	FB B WDQS<6>	67 69 76
	FB_D_WDQS3	GDDR3_46SF	GDDR3_DQS	FB B WDQS<7>	67 69 76
	FB_D_RDQS0	GDDR3_46SE	GDDR3_DQS	FB B RDQS<4>	67 69 76
	FB_D_RDQS1	GDDR3_46SE	GDDR3_DQS	FB B RDQS<5>	67 69 76
	FB_D_RDQS2	GDDR3_46SE	GDDR3_DQS	FB B RDQS<6>	67 69 76
	FB_D_RDQS3	GDDR3_46SE	GDDR3_DQS	FB B RDQS<7>	67 69 76
	FB_D_DQ_BYTE0	GDDR3_46SF	GDDR3_DATA	FB B DQ<39..32>	67 69 76
	FB_D_DQ_BYTE1	GDDR3_46SF	GDDR3_DATA	FB B DQ<47..40>	67 69 76
	FB_D_DQ_BYTE2	GDDR3_46SF	GDDR3_DATA	FB B DQ<55..48>	67 69 76
	FB_D_DQ_BYTE3	GDDR3_46SF	GDDR3_DATA	FB B DQ<63..56>	67 69 76
	FB_D_DQM0	GDDR3_46SE	GDDR3_DATA	FB B DQM L<4>	67 69 76
	FB_D_DQM1	GDDR3_46SE	GDDR3_DATA	FB B DQM L<5>	67 69 76
	FB_D_DQM2	GDDR3_46SE	GDDR3_DATA	FB B DQM L<6>	67 69 76
	FB_D_DQM3	GDDR3_46SE	GDDR3_DATA	FB B DQM L<7>	67 69 76

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	(CK505_D0T96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30 71
	CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30 71
	LVDS_L_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P	72 74
		LVDS_100D	LVDS	LVDS_L_CLK_N	72 74
	LVDS_L_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<2..0>	72 74
		LVDS_100D	LVDS	LVDS_L_DATA_N<2..0>	72 74
		LVDS_100D	LVDS	LVDS_L_DATA_P<3>	71 72
		LVDS_100D	LVDS	LVDS_L_DATA_N<3>	71 72
	LVDS_U_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P	72 74
		LVDS_100D	LVDS	LVDS_U_CLK_N	72 74
	LVDS_U_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<2..0>	72 74
		LVDS_100D	LVDS	LVDS_U_DATA_N<2..0>	72 74
		LVDS_100D	LVDS	LVDS_U_DATA_P<3>	71 72
		LVDS_100D	LVDS	LVDS_U_DATA_N<3>	71 72
	TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	72 78
	TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N	72 78
	TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>	72 78
	TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>	72 78
	VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	71 78
	VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	71 78
	VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	71 78
		VGA_50S	VGA	GPU_VGA_R	71 72
		VGA_50S	VGA	GPU_VGA_G	71 72
		VGA_50S	VGA	GPU_VGA_B	71 72
		VGA_50S	VGA	GPU_TV_C	71 72
		VGA_50S	VGA	GPU_TV_Y	71 72
		VGA_50S	VGA	GPU_TV_COMP	71 72
	VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	72 78
	VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	72 78

GPU (G84M) Constraints

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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